Status of Front End Chip Development for the ALICE Pixel Detector

Presented by W. Snoeys[1] for the ALICE collaboration
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ABSTRACT

The ALICE pixel development strongly builds on the experience gained at CERN in the WA-97 [1] and NA-57 [2] experiments from operating a full pixel system developed in close collaboration with the RD-19 collaboration [3]. Two chips have been designed as prototypes for the ALICE pixel detector. Both contain front end and digital readout circuitry for 130 pixels. The first one, implemented in a commercial 0.5 μm technology, contains a newly designed front end capable of handling large detector leakage currents and large leakage current variations (~ 100 nA) with minimal threshold variation (~1 %). Special layout techniques studied in more detail in the RD-49 collaboration [4] were used to increase the radiation tolerance of the circuits. At an X-ray dose rate of 4 krad/min the chips started to degrade significantly only after 600 krad. In an ionizing particle beam significant degradation set in after 1.7 Mrads administered in approximately two days.

Density considerations pushed to go to even deeper submicron for the next prototype. It was designed in 0.25 μm standard CMOS, the front end and discriminator have been modified to avoid using large enclosed NMOS devices for current mirroring. As a result of this and the smaller feature size the front-end now measures only 120 μm on a 50 μm pitch compared with about 270 μm on the same pitch in the old design. Moreover, a 3-bit threshold adjust has been added. 2 different counter designs have been implemented which should replace the delay line used in the Omega3 chip. The static counter measures 40 μm by 60 μm whilst the dynamic counter measures only 40 μm by 35 μm. It is now clear that the functionality required of the Alice pixel cell can be implemented within 300 μm using this technology.

[1] F. Antinori et al. : "First Results from the 1994 Lead Beam run of WA97", Nucl. Phys. A590 (1995) 139c-146c.

[2] F. Antinori et al.: "Study of strange and multi-strange particles in ultrarelativistic nucleus-nucleus collisions" CERN/SPSLC/96-40 SPSLC/P300.

[3] F. Anghinolfi et al. : "A 1006 element hybrid silicon pixel detector with strobed binary output", IEEE Trans. Nucl. Sci. NS-39 (1992) 650, and E. H. M. Heijne et al. : "LHC1 : A semiconductor pixel detector readout chip with internal, tunable delay providing a binary pattern of selected events", Nucl. Instr. Meth. A383 (1996) 55-63, and RD-19 Progress reports 1992-1997.

[4] P. Jarron et al., RD49 Proposal CERN/LHCC 97-2, January 1997, and first status report CERN/LHCC 97-63, December 1997, and G. Anelli et al. : "Total Dose behavior of submicron and deep submicron technologies", Proc. of the Third Workshop on Electronics for LHC Experiments, London, September 22-26, 1997 (CERN/LHCC/97-60)

Status of Front end development for the ALICE Pixel Detector

Presented by :
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Fermilab Pixel Workshop, May 7-9, 1998

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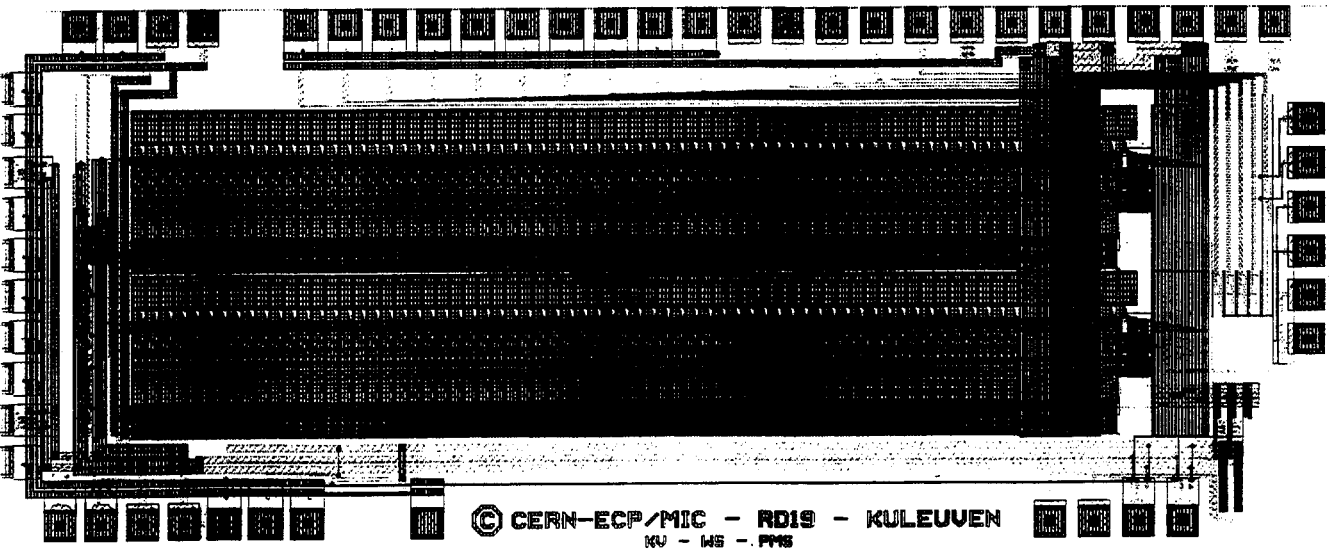
OVERVIEW

- **LHC2TEST in 0.5 micron CMOS electrical and irradiation results**
- **Photon Counting Chip (PCC) threshold adjust**
- **New submission ALICE2TEST**
- **Conclusions**

LHC2TEST in 0.5 micron

- Contains 2 columns of 64 pixels + 1 test pixel with analog outputs)
- Each pixel element contains :
  - test and mask
  - front end with capability to collect holes or electrons, and detector leakage current compensation
  - readout logic (strobe but no delay line)
- laid out in radiation tolerant layout

W. Snoeys - CERN - EP - MIC



LHC2TEST

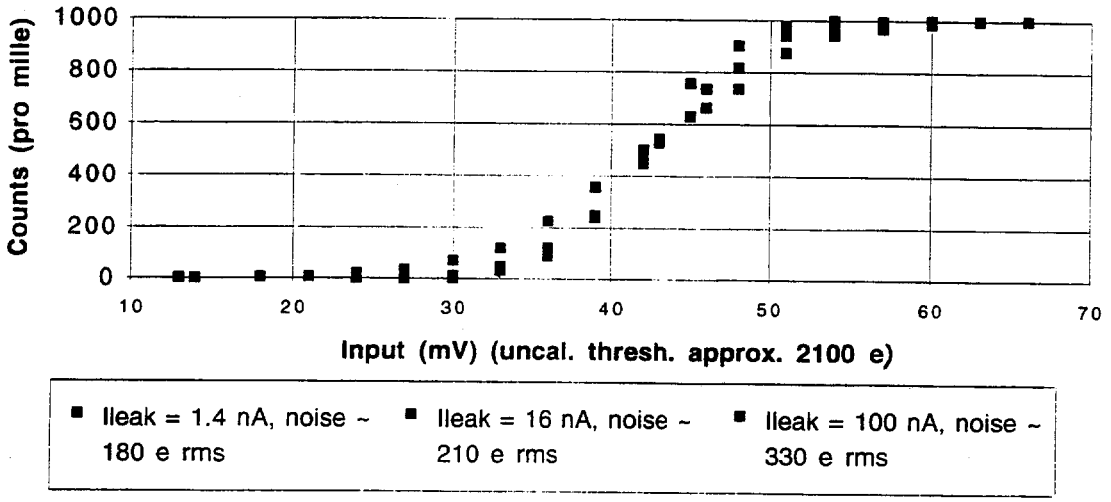
Pixel Readout Prototype in Radiation Tolerant Layout in Commercial Submicron Technology

CERN ECP-MIC RD19 - RD49 ALICE

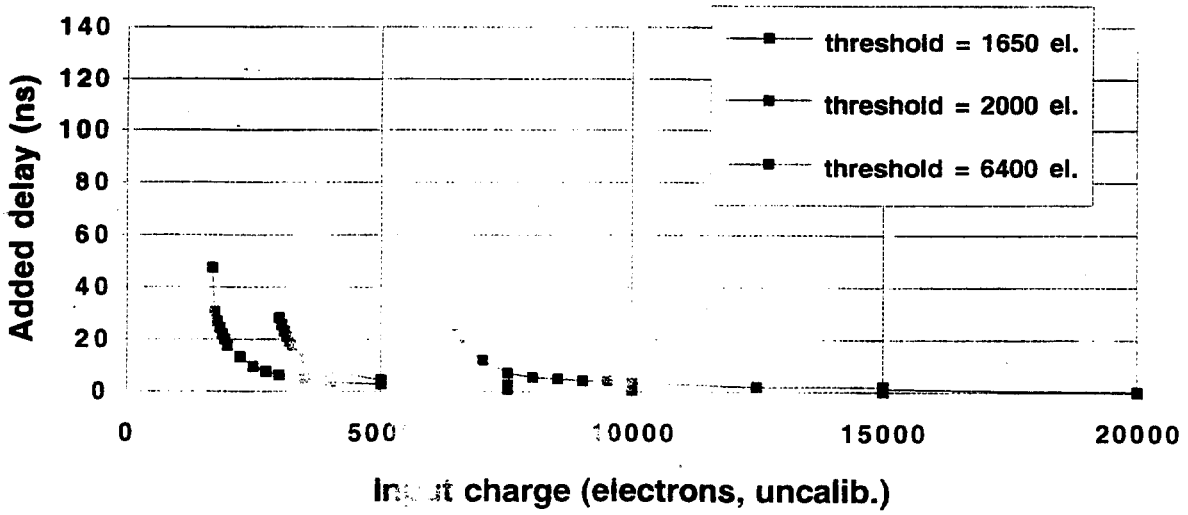
(Mietec 0.5 μm)

2 x 65 pixelcells (50 x 420 μm²)

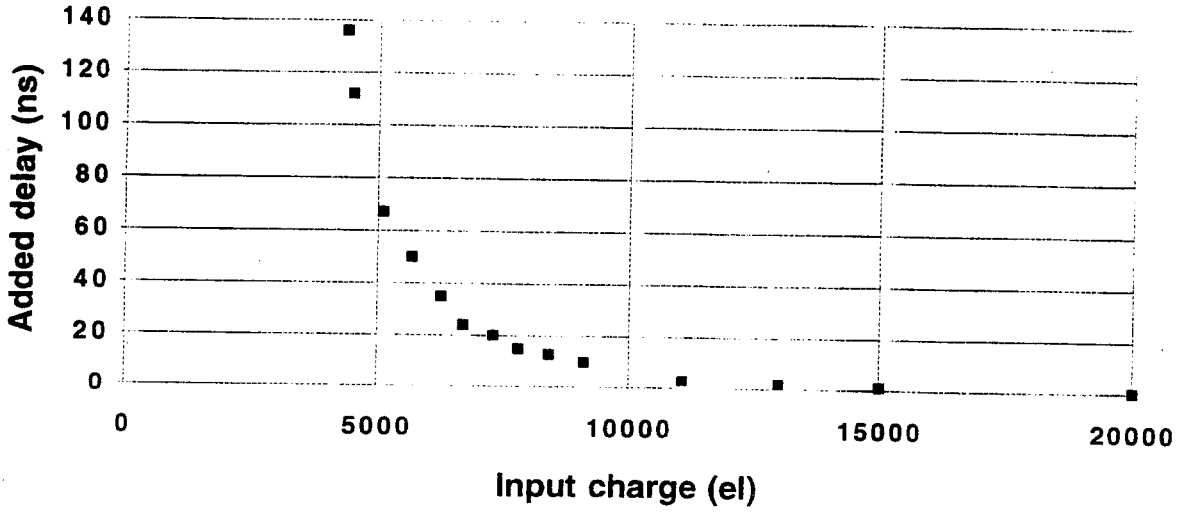
Threshold dependence on leakage current per pixel



Timewalk measurement LHC2TEST



Timewalk measurement LHC1



LHC2TEST electrical results

- for a detector leakage current increase of 1 to 200nA :
  - threshold variation ~ 1%
  - noise increase from about 200e RMS to 400e RMS for holes, and to 350e RMS for electrons.
- threshold variable between 2000 to 15000 holes or electrons
- threshold spread too large (400 - 500 e RMS)
- timewalk within 25 ns for only a few 100 electrons above threshold

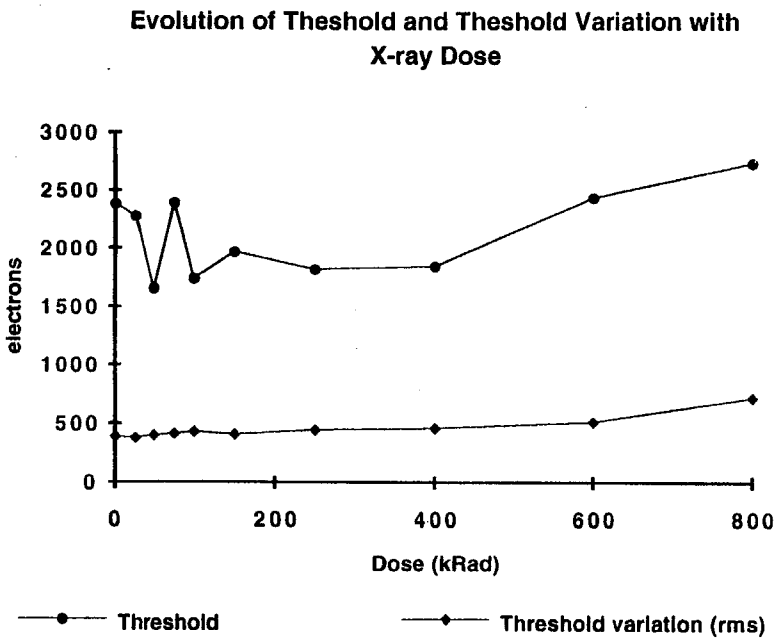
LHC2TEST
Radiation Tolerance

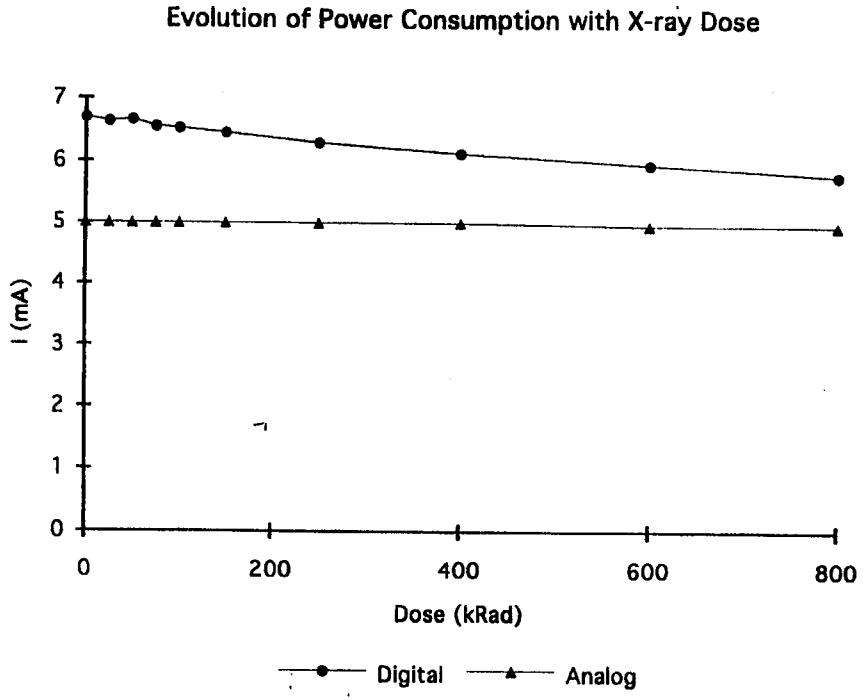
- Irradiation tests done with 10 keV X-rays, Gamma ^{60}Co, 6.5 MeV protons, and electrons in NA50
- No large increase in supply currents with dose => rad tolerant layout techniques prevent leakage
- Serious degradation (= severe pixel threshold increase) sets in only after ~600 krads with Xrays and ~1 Mrad or higher for the other sources (e.g. 1.7 Mrad for NA 50 beam)

LHC2TEST
Radiation Tolerance

- Main reason for threshold increase is shaper response decreases sharply in amplitude (verified on analog outputs)
- Significant recovery (annealing) after a relatively short time

W. Snoeys - CERN - EP - MIC


Evolution of Theshold and Theshold Variation with X-ray Dose
electrons
3000
2500
2000
1500
1000
500
0
0
200
400
600
800
Dose (kRad)
Threshold
Threshold variation (rms)


Evolution of Power Consumption with X-ray Dose
I (mA)
7
6
5
4
3
2
1
0
0
200
400
600
800
Dose (kRad)
Digital
Analog

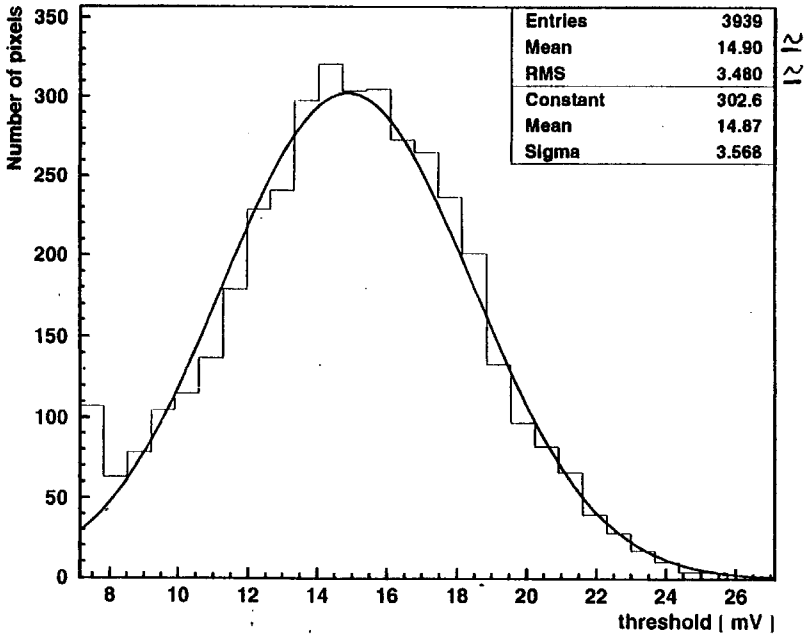
10 keV Xray irradation of LHC2TEST

	Average Threshold	Threshold variation RMS	Average Noise	Noise variation RMS	Valid Pixels
400 krad					
before	2262	431	216	31	127
immediately after	2091	445	237	26	125
after 1 day at RT	2173	439	237	27	126
after 1 week at 100 C	1546	373	239	21	90
600 krad					
before	2243	431	218	26	130
immediately after	2554	560	263	20	130
after 1 day at RT	2357	483	237	21	129
after 1 week at 100 C	2234	447	226	16	128
800 krad					
before	2276	413	224	18	124
immediately after	4342	1657	372	69	130
after 1 day at RT	2534	629	265	25	126
after 1 week at 100 C	1689	475	261	28	90

PHOTON COUNTING CHIP

3BIT THRESHOLD ADJUST

Threshold Distribution



≈ 1396
≈ 326

88

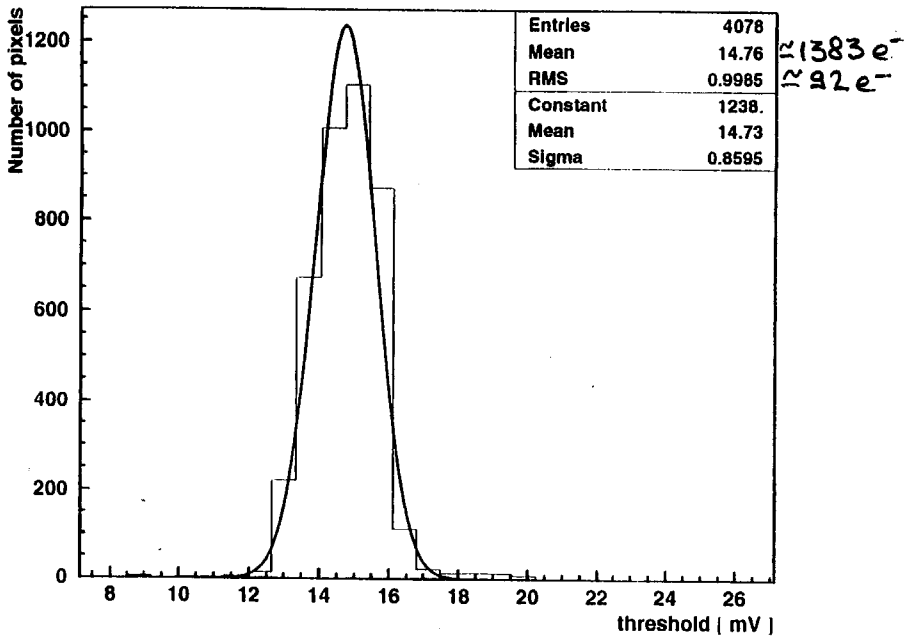
BEFORE ADJUST

RD-19

M. CAMPBELL

PHOTON COUNTING CHIP

Threshold Distribution



≈ 1383 e⁻
≈ 92 e⁻

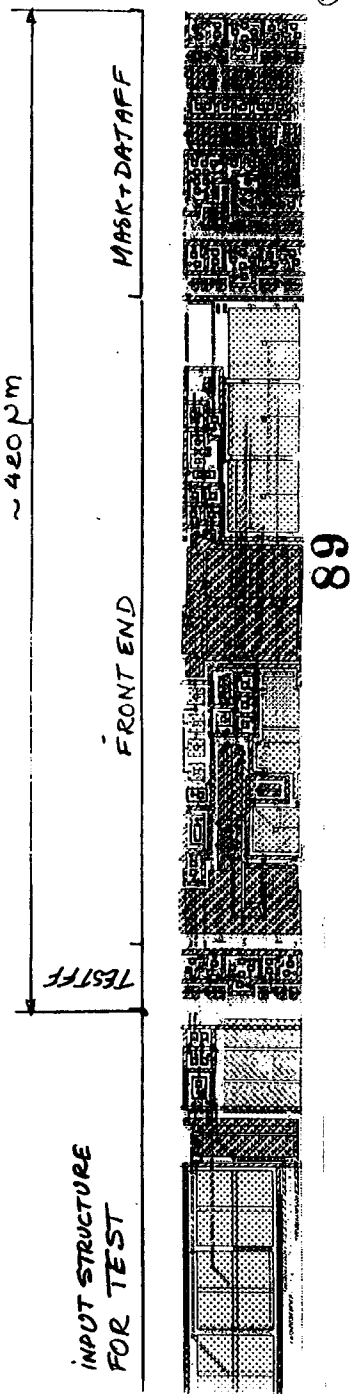
AFTER ADJUST

RD-19

H. CAMPBELL
F. PERNIGOTTI

LHC2TEST / ALICE 1 TEST

BIG CURRENT MIRROR ELIMINATED IN ALICE1TEST



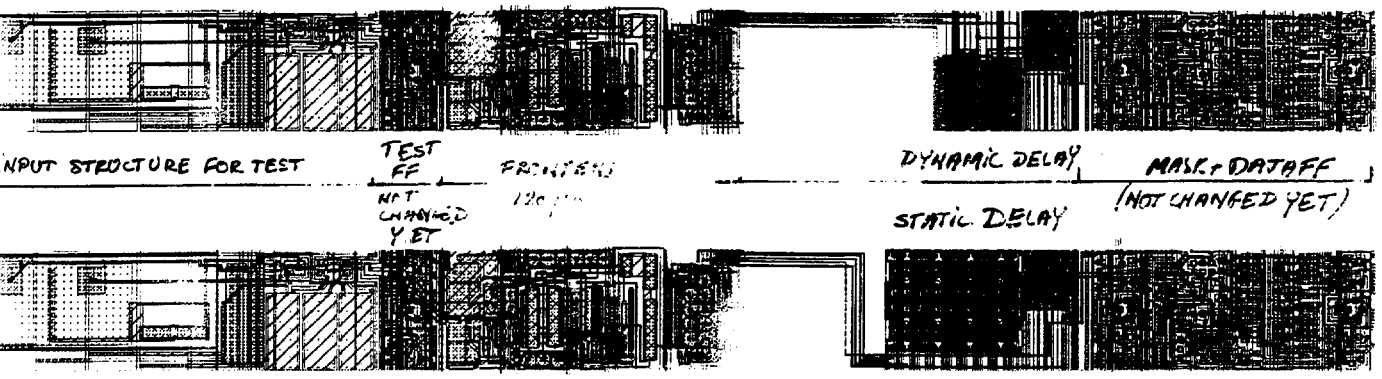
ALICE2TEST in 0.25 micron CMOS

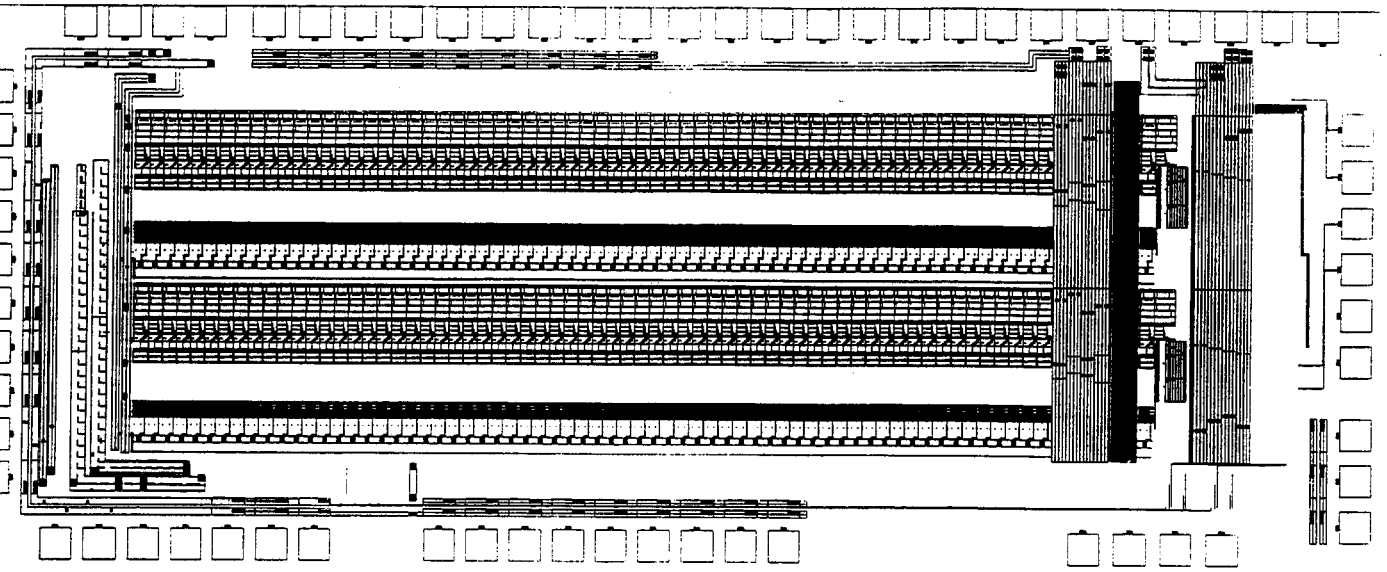
- Contains 2 columns of 64 pixels + 1 test pixel with analog outputs)
- Each pixel element contains :
  - test and mask
  - front end with capability to collect holes or electrons, and detector leakage current compensation, and threshold adjust (local digital storage not yet included)
  - digital counter - based delay line two versions : static and dynamic
  - readout logic
- laid out in radiation tolerant layout

ALICE2TEST

- static a dynamic delay based on counter
  counter itself (without control)
  static: $40 \times 60 \mu m^2$
  dynamic: $40 \times 35 \mu m^2$

- clear we will be able to fit full ALICE pixel in 300μm long pixel (50μm pitch)





ALICE2 TEST
submitted in
0.25 μm
technology

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CONCLUSIONS

- **LHC2TEST (0.5 um) excellent results regarding timewalk, detector leakage current compensation and radiation tolerance BUT insufficient density and relatively large threshold variation.**
- **Therefore ALICE2TEST (0.25 um), expected back early July, density sufficient to implement ALICE pixel in 50 x 300 um, threshold adjust added to improved front end (principle of adjust demonstrated on PCC)**
- **Full ALICE chip to be submitted by the end of the year.**

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Readout chip development for the ATLAS pixel detector

Thorsten Kuhl
Physikalisches Institut Bonn

Contents:

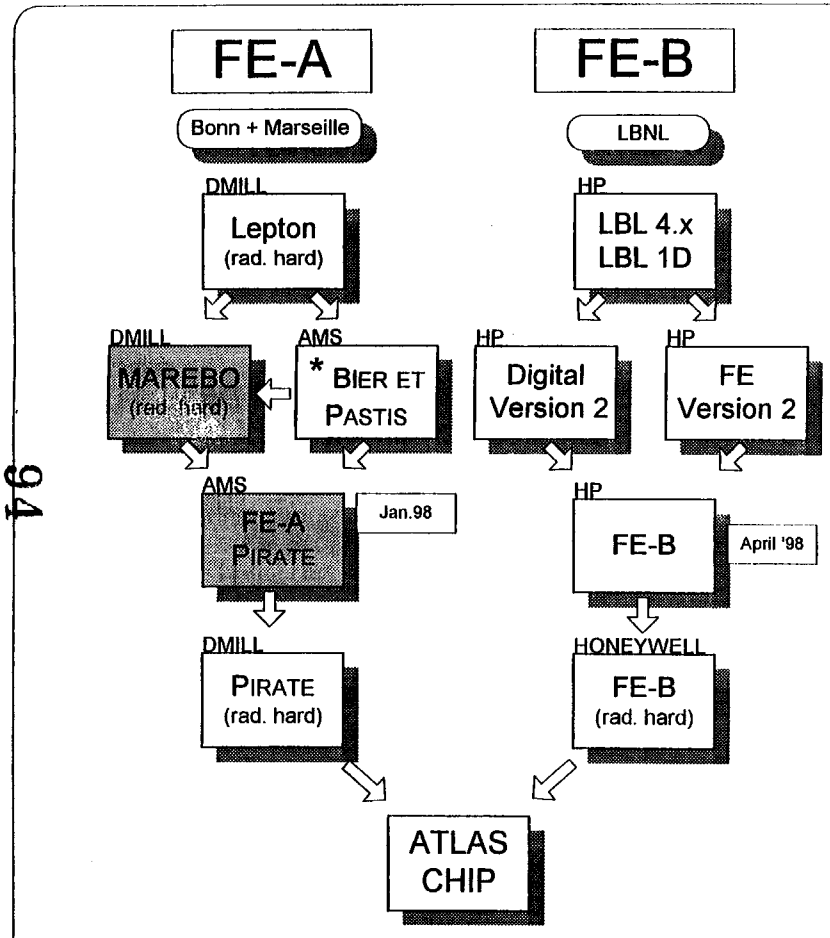
- Requirements for pixel frontend electronics at LHC
- **Pi**xel **R**eadout Chip for the **ATLAS E**xperiment (PIRATE)
- Radiation hard development (MAREBO)
- Summary

Requirements for ATLAS pixel electronics

1. Pixel size of 50 x 300 μm^2
   achieve required spatial resolution
2. Amplifier noise of < 200 e^- e.n.c.
   get low noise hit rate at low threshold, needed to detect small charges after radiation damage of sensor
3. Threshold uniformity of typ. 200 e^- rms
   required to set low global threshold
4. Power consumption of <50 µW per pixel
   reduce cooling effort (-> radiation length!)
5. Timing precision of 25 ns
   uniquely associate hits to bunchcrossings
6. Leakage current tolerance of up to 100nA
   operate with DC-coupled detectors
7. Zero supression
   read only hit pixels
8. Trigger selection
   buffer events for 80-100 crossings until T1 trigger occurs
9. Radiation hardness
   survive 20-30 Mrad in 10 years of operation
10. Testability
    test every pixel before module assembly

Note: pixel occupancy is < 10^{-4} hits / crossing

Readout chip development history



*) B&P was the first chips which fulfils the ATLAS analog requirements

Pixel Readoutchip for ATLAS PIRATE

Universität Bonn / CPP Marseille

(received & tested jan. 1998)

direct successor of the BEER & PASTIS chip

- 18 x 160 pixels (50 µm x 400 µm)
- preamplifier for n/n detectors
- threshold adjust for every pixel (3 bit DAC)
- time over threshold information
- 8-bit DAC's for internal currents
- serial command protocol
- complete 40 MHz digital logic for ATLAS
- serial data readout
- works under full luminosity conditions

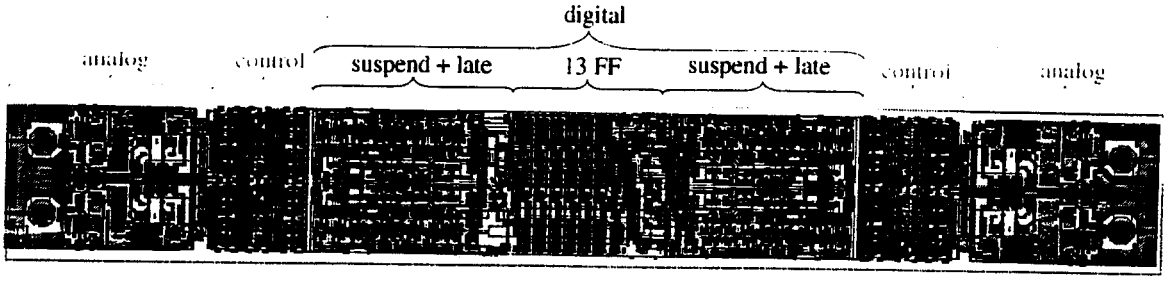
FNAL Pixel Workshop 98
Thorsten Kuhl, PI Bonn

- ACTIVE PART

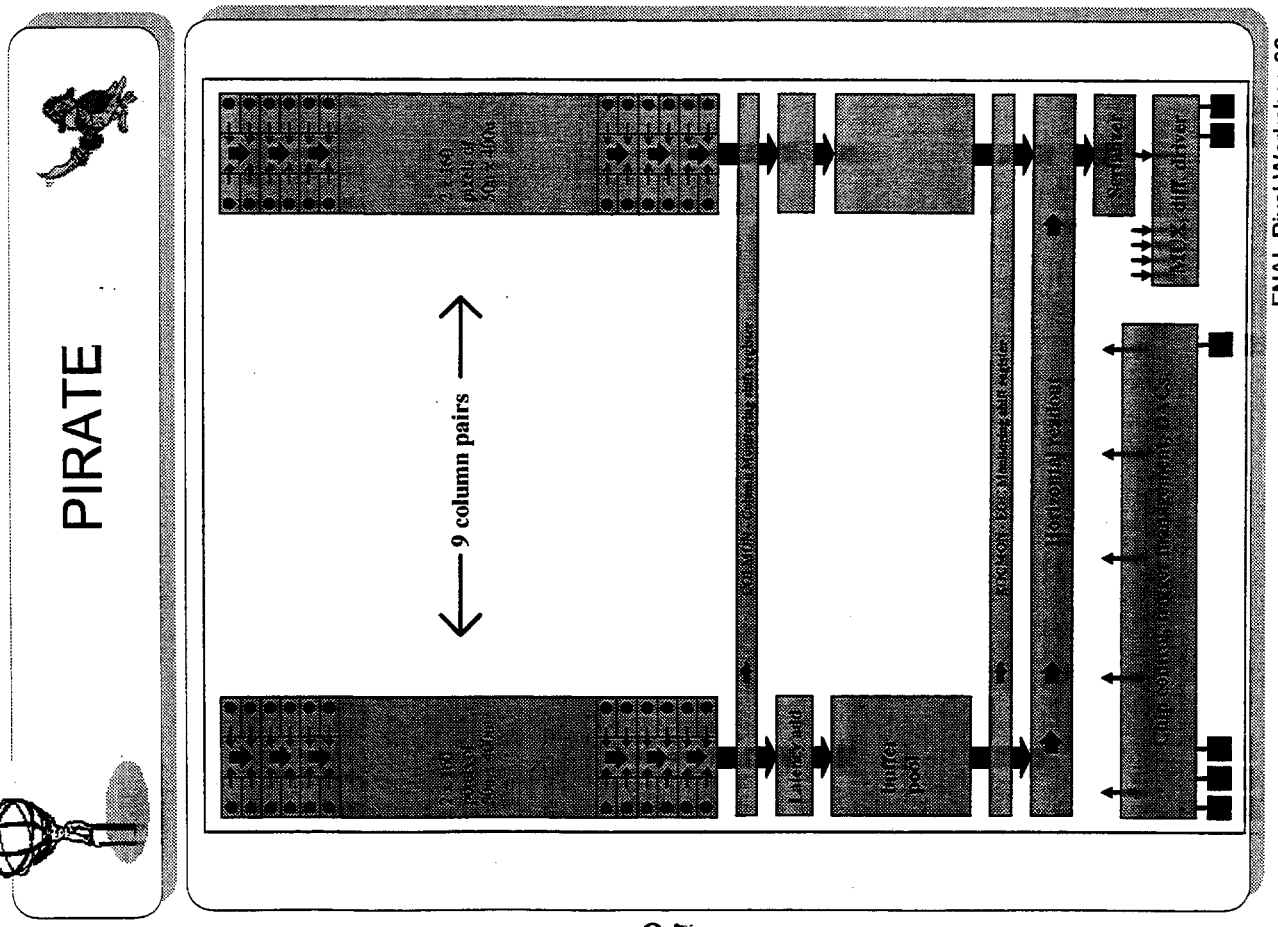
☞ ***Analog part (140u)***
include 3 bits DAC for tuning

☞ ***Control part (80u)***
mask, inject .....

☞ ***Digital part (180u)***
1 RO part for 4 contiguous pixels
7 bits of address
2 bits late
1 bit rise (for ToT information)
1 bit Up/Down (for group)
1 bit Left/Right (for group)



- pixel size : 400µm * 50µm



Digital performance

Full simulation of the FE-architecture

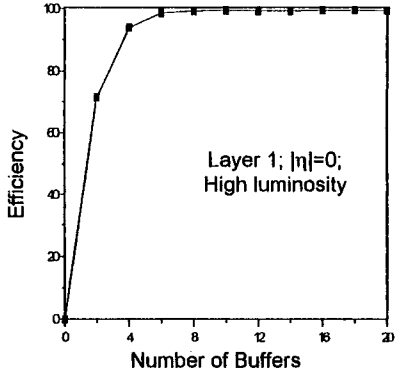
- simulation of digital part
- cluster taken from full detector monte carlo
- random tracks

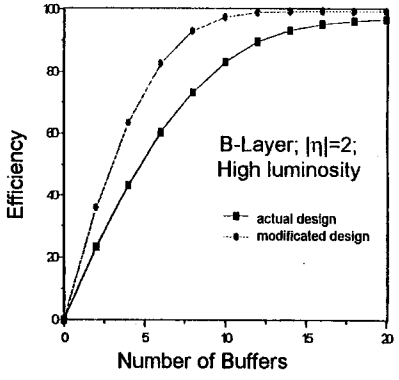
Inefficiencies can occur by:

- occupancy of single pixel
- collisions in the shift register
- buffer overflow

Results ($\mathcal{L}=10^{34}cm^{-2}s^{-1}$):

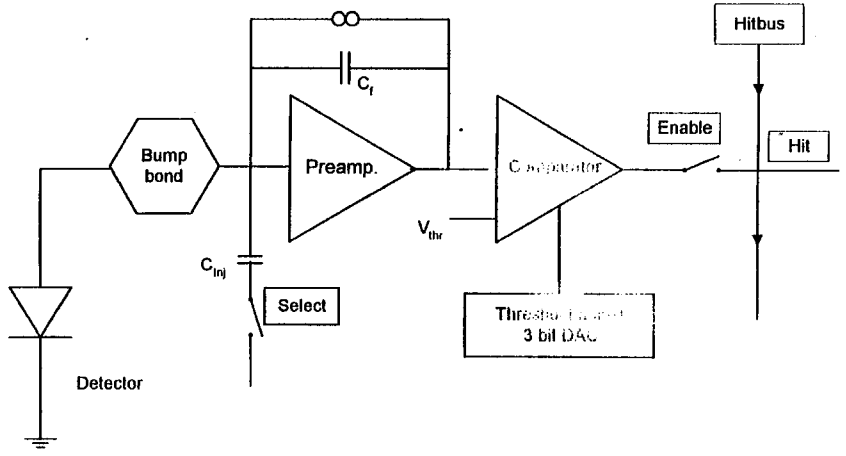
- at $|\eta|=0$, Layer 1: $\varepsilon >> 99$ % with 8 buffers
- at $|\eta|=2$, B-Layer: $\varepsilon > 95$ % with 16 buffers;
  with small modifications: $\varepsilon > 99$ % with 12 buffers
- general: architecture can cope well with highest LHC luminosity





Analog part of the PIRATE

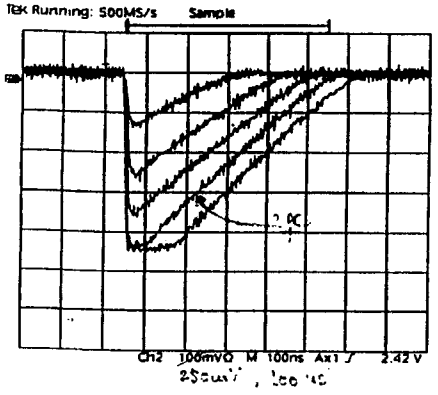
schema of analog part



- fast amplifier with novel DC feedback
- threshold adjust with 3 bit DAC in **every pixel**
- Enable: masking pixel
- hitbus for monitoring
- linear time over threshold (TOT) behaviour
- chopper for test injection on chip
- internal 8 bit DACs for bias currents

Analog signals from preamplifier

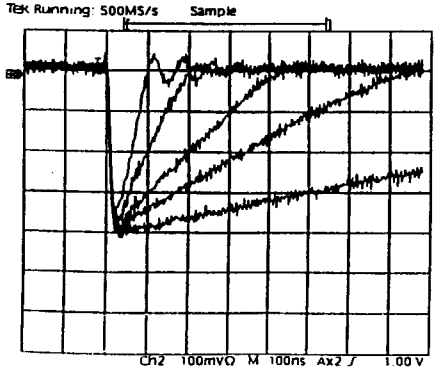
- Preamplifier operated at 30 uW
- Feedback in amplifier is a constant current source



Q_{in} = 0.5, 1, 1.5,... fC

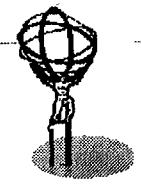
$C_{feedback}$ = 1.7 fF

~ m.i.p. ≙ 2V signal at output

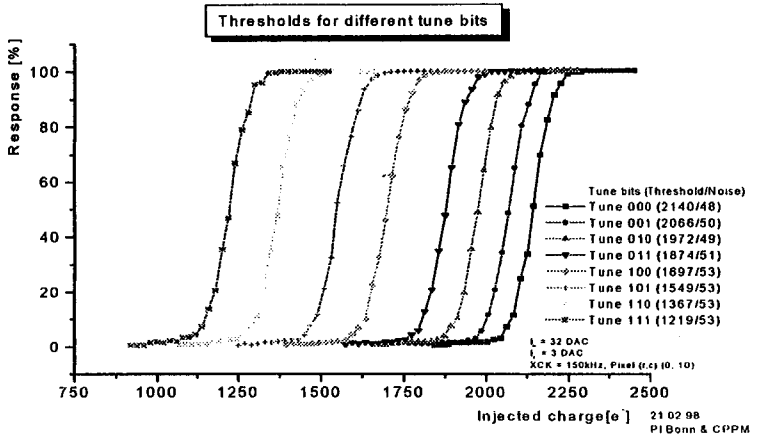


Variation of feedback current:

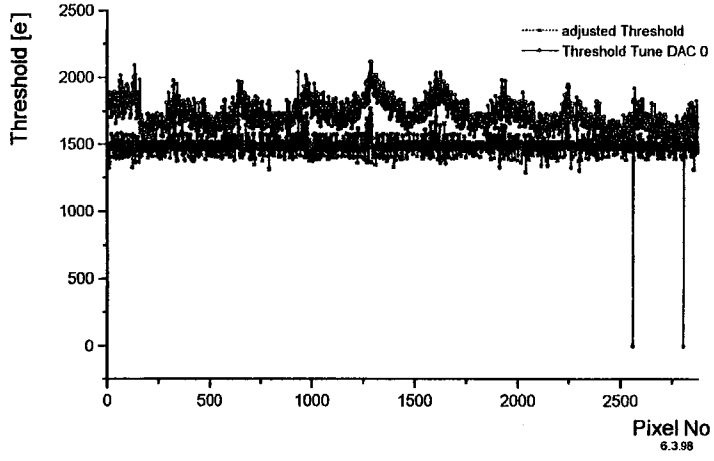
- very good stability
- small shaping loss
- high leakage tolerance

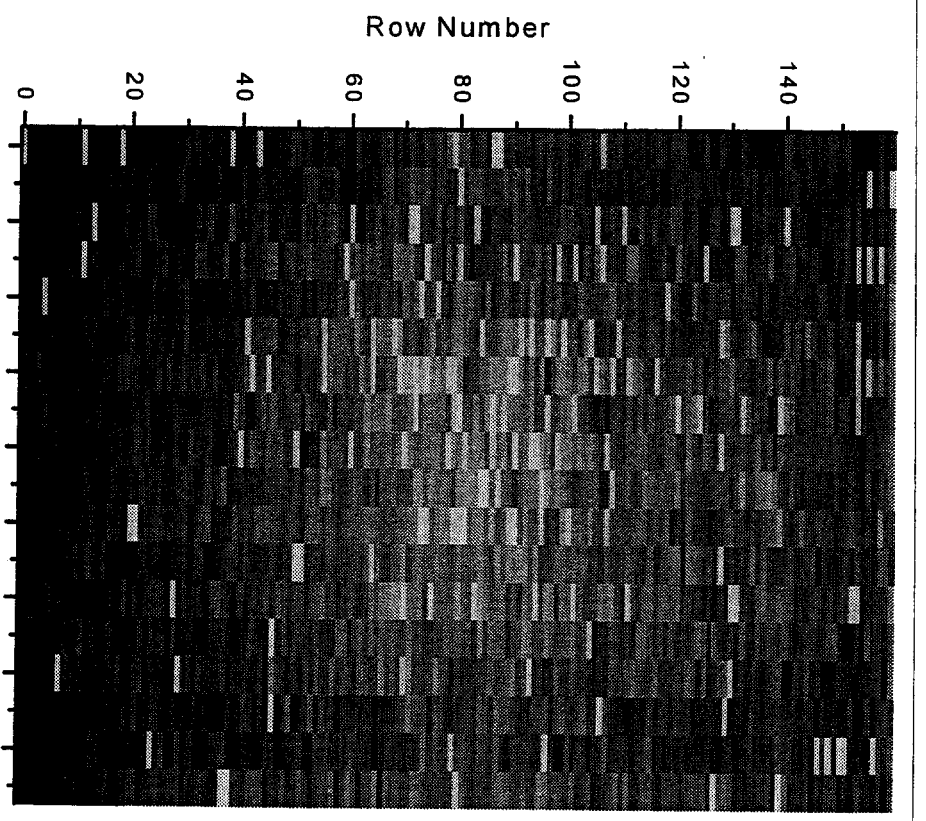


Threshold adjust



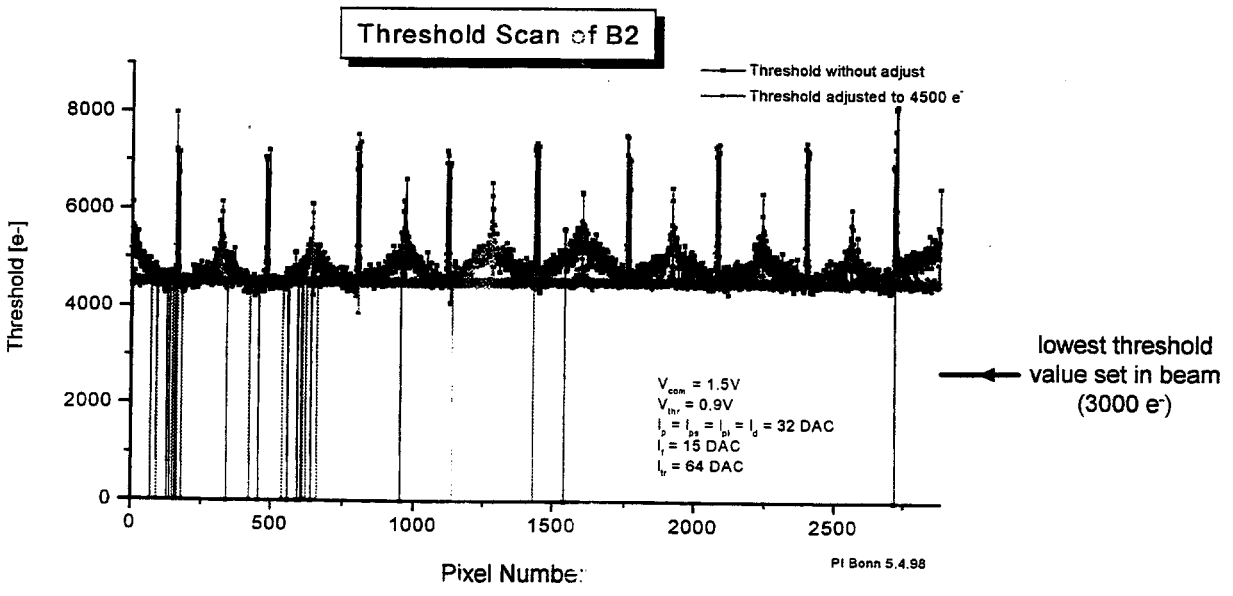
Threshold scan without/with adjust



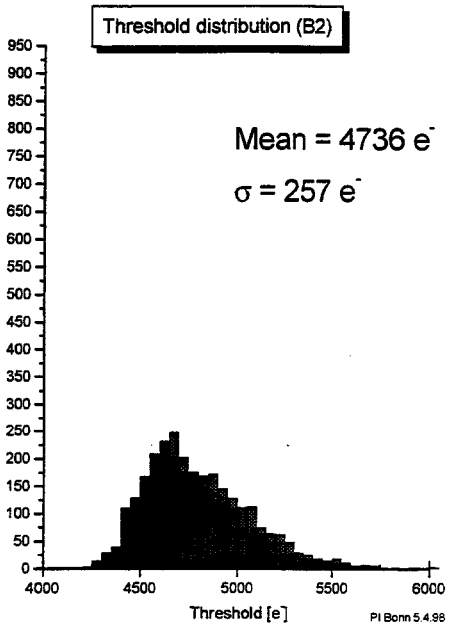


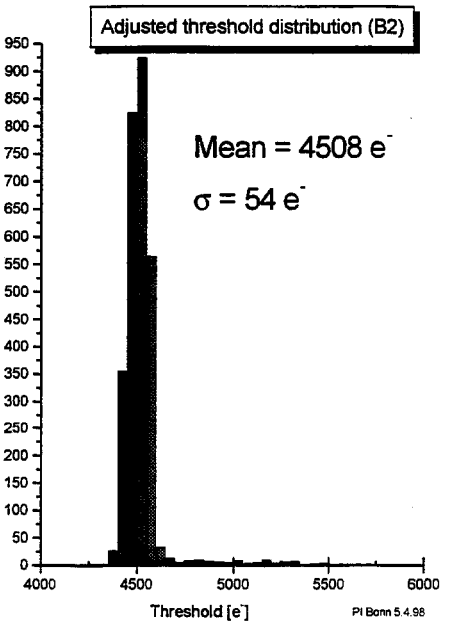
Hit map from Am^{241} source

Threshold scan with detector

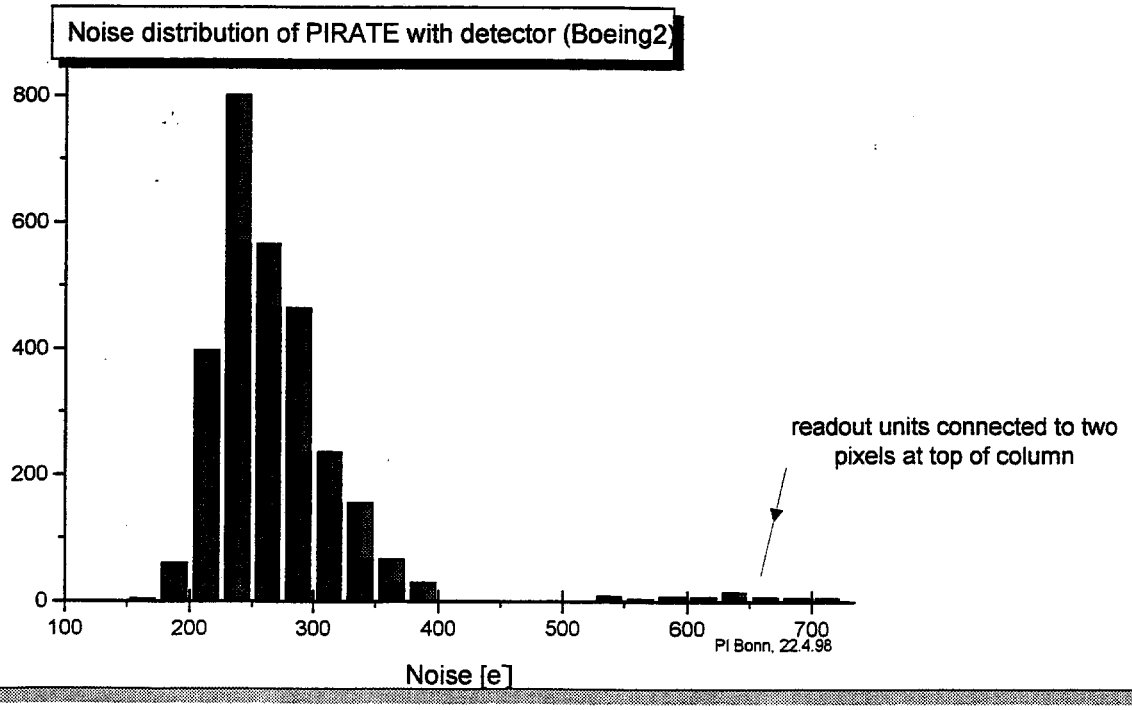


Threshold distributions





Noise

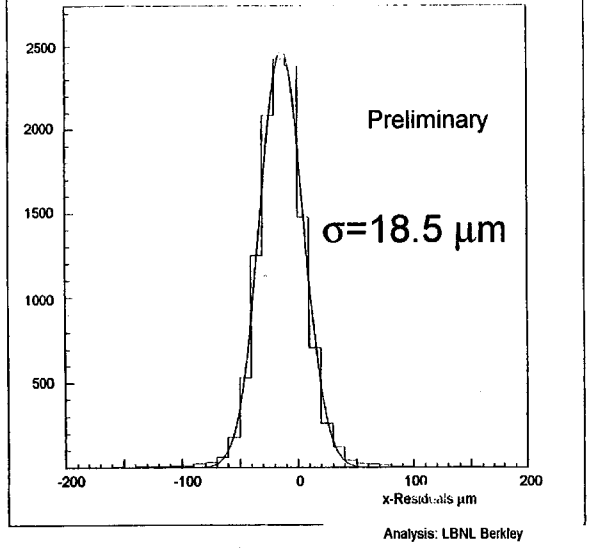


Test beam

First test beam 01.04.98-21.04.98
(CERN, 50 GeV Myons)

- test of several chips
- different detector configurations
- test system works well
- sucessfull data taking

PIRATE (IZM4) in test beam (April '98)

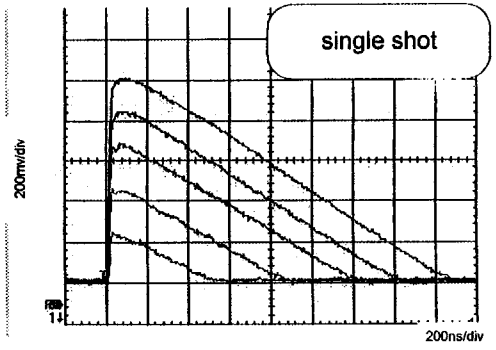


Analysis: LBNL Berkley

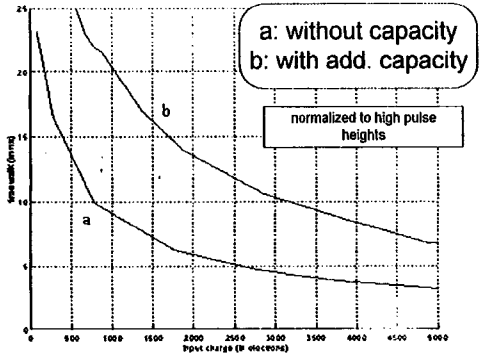
MAREBO

Radiation hard readout chip with reduced digital part.

Preamplifier signals single channel



Timewalk behaviour



Summary and outlook

PIRATE works well and has been successfully operated in beam

1) operation @ 3000 e^- setting in beam
2) at full ATLAS speed (40 MHz)
3) low noise (250 e^- with detector)
4) low treshold variation (< 50 e^- after adjust)
5) successfully bumped to sensors
6) radiationhard FE has timewalk <1000 e^- @ 200fF
7) serial ATLAS protocol for control and readout works @ 40 MHz
8) poor chip yield

Applications of the ISPA-tube in nuclear medicine and biology

C. D'Ambrosio1, F. de Notaristefani2, T. Gys1, E. Heijne1, H. Leutz1,
D. Piedigrossi1, D. Puertolas1,2, E. Rossi1
1 CERN, 2 INFN Section of Rome

abstract:

The Imaging Silicon Pixel Array (ISPA)-tube [1] is a position-sensitive photon detector based on the hybrid technology [2]. It consists of a vacuum-sealed cylinder with an optical entrance window on which is evaporated a photocathode. A potential difference (20 to 25 kV) is applied between the photocathode and a silicon chip anode. The chip anode is based on the Omega 2 and LHC1 chips, developed by the RD-19 collaboration [3,4]. It consists either of one detector plane divided into 1024 pixel diodes (500 çm x 75 çm in size) and one electronics plane also divided into 1024 equally-sized electronic pixels (Omega 2 chip) or of one detector plane divided into 2048 pixel diodes (500 çm x 50 çm in size) connected to 2048 equally-sized electronic pixels (LHC1). Each detector pixel is directly bump-bonded to its front end-electronics pixel. The binary response of individual pixels thus provides a space information and allows 2D-imaging. An important feature of the tube is the possibility to trigger it internally: the analog signal from the bias contact of the detector chip, arising from the photoelectron pool generated by each event in the scintillator, can be appropriately amplified and shaped. It provides a fast (10 ns), global information allowing an easy energy calibration and an energy window selection. All events falling inside this energy window start the gating and readout of the tube.
For nuclear medicine, we built an ISPA-camera for g-rays by coupling a YAP(YalO3(Ce)) planar crystal or a YAP-crystal array (consisting of 0.6 x 0.6 mm2 optically-separated YAP-elements) to an ISPA-tube [5]. Presently, using a YAP-crystal array containing 0.3 x 0.3 mm2 elements we achieve an improved spatial resolution (FWHM) of 100 çm at 122 keV g-energy, the overall spatial resolution of the system being dictated by the crystal element size. The energy resolution of the system can be made as high as 21% at FWHM for 122 keV photons, allowing rejection of Compton scatters, while still providing a good spatial resolution (~500 çm).
For biology and in particular autoradiography, we built a beta camera made of a thin scintillator placed onto the ISPA-tube window. Resolutions down to 100 çm have been achieved and beta detection sensitivities measured with calibrated Tritium and Carbon-14 Amersham calibrated sources. Microslices of mouse brain labelled with Sulfur-35 have been imaged and analyzed.
Last development, which consists in a new electrostatic focussing tube (demagnification ~4) containing an LHC1 chip, as well as future developments, both for the tube and for a specific chip, will be finally presented.

References
[1] T. Gys et al., "A new position sensitive photon detector based on an imaging silicon pixel array (ISPA- tube)", Nucl. Instr. and Meth. in Physics Res., vol. A355, 1995, p. 386.
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[3] E. H. M. Heijne et al., "Development of silicon micropattern pixel detectors", Nucl. Instr. and Meth in Physics Res., A348, 1994, p. 399 .
[4] E.H.M. Heijne et al., "LHC1: A semiconductor pixel detector readout chip with internal tunable delay providing a binary pattern of selected events", Nucl. Inst. and Meth. in Phys. Res., A383 (1996) 55.
[5] D. Puertolas et al., "An ISPA-camera for g-rays in nuclear medicine", Nuclear Physics B (Proc. Suppl.) 61B (1998) 644.

Fermilab 7 May 1998

C. D'Ambrosio

The ISPA – Tube in Medicine and Biology

Working Principle

Applications of the ISPA (Imaging Silicon Pixel Array) tube

- γ-camera for SPET
- β-camera for β-radiography

Conclusions and Future Outlook

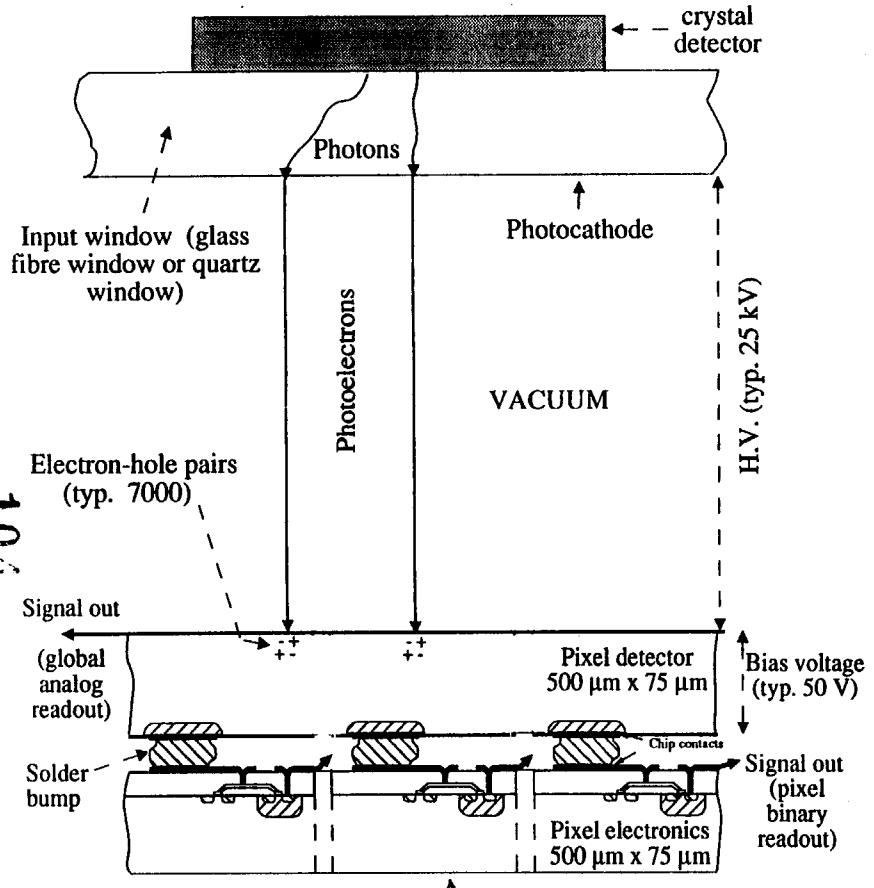
People involved in our R&D :

Different groups at CERN and INFN Rome

Industrial partners like:

DEP, Edgetek, GEC - Marconi, Preciosa - Crytur

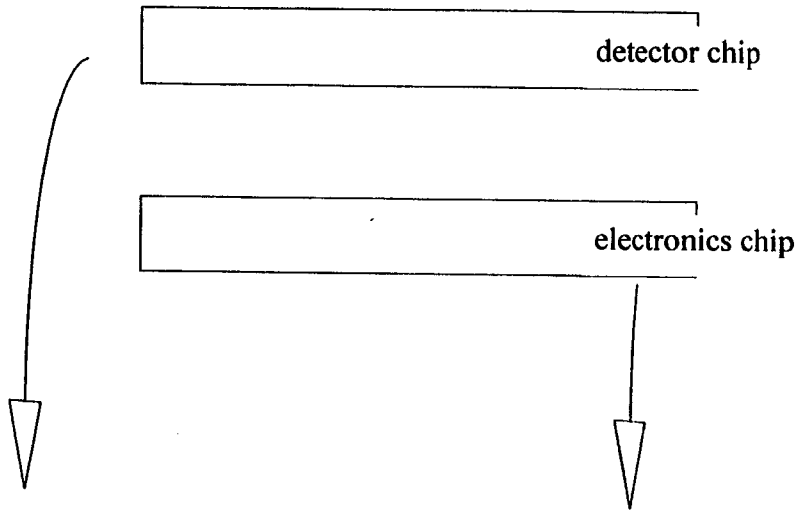
Position-sensitive photon detection with an ISPA-tube



pixels chip is Ω1, Ω2, Ω3 developed by RD-19 and CERN-MIC group

CERN-PPE/OF
LAA-RD7
CERN-ECP/MIC
RD19

The Self – Triggering Principle



Fast, analogic and global information	Pixel signals out (with present chip, pixel response is binary)
Trigger for strobe	Precise space information
Immediate calibration in photoel. or energy	2-D imaging
Selection of a window in energy possible	

The ISPA Tube is a photon- and position- sensitive optoelectronic device.

It is fast : its "shutter" is as fast as nanoseconds;
It can stand high readout rates (at present 1 Mhz)
It features high spatial resolution: as low as 50 μm;
Its photocathode has a high Q. E. : ~25% in the near UV
It is photon sensitive with a Single El. Resolution ~ 20 %

Our goal is to have a "video camera" sensitive to photons from near-infrared to γ-rays, but also to charged particles, β-rays or neutrons.

The idea is to just use a "suitable lens" (or active medium) for our camera to convert a certain process into a photoelectronic image.

For Scintigraphy applied to human organs, requirements are:

- High counting efficiency (decrease the quantity of radio-tracer),
- Spatial resolution around 1 mm FWHM (better image definition),
- Energy resolution around 20% FWHM (background rejection),
- Event rate ~1 MHz/cm^2
- Readout rates ~10 kHz/ cm^2
- Large active surface (50 cm^2 to 500 cm^2)

For β – autoradiography, main requirements are:

- Linearity,
- High counting efficiency for a wide range of beta energies,
- High spatial resolution (less than 100 μm FWHM)

Carmelo D'Ambrosio, CERN/EP-TA2

γ - detection

for medical applications ^{99}Tc ~ 140 keV gamma energy

The active medium consists in either :

a YAP – crystal thin plate (1 to 2 mm) or

a YAP – array

(from 300 μm to 600 μm square sizes and 10 mm length)

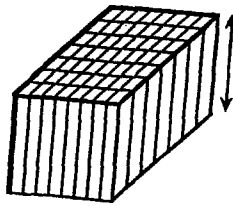
Results

- Spatial resolution: from 250 μm to 700 μm (FWHM)
- Energy resolution (at 122 keV): from 20% to 50% (FWHM)
- Detection efficiency (without coll.) from 20% to 90% (at 122 keV)

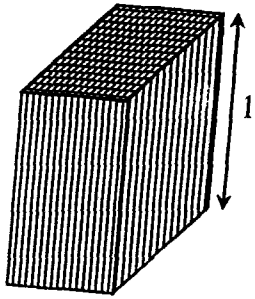
YAP crystal detectors *
(emits light around 380 nm)

YAP-plate

18 % eff. @ 122 keV



YAP-array1
600 x 600 μm^2 crystal elements
62 % eff. @ 122 keV



YAP-array2
300 x 300 μm^2 crystal elements
86 % eff. @ 122 keV

YAP emission peaks at ~365 nm

@ 122 keV —> photoeffect : 63 %
Compton : 37 %

Our YAP crystal detectors are produced by Preciosa Krytur, Tournov, Czech Republic.

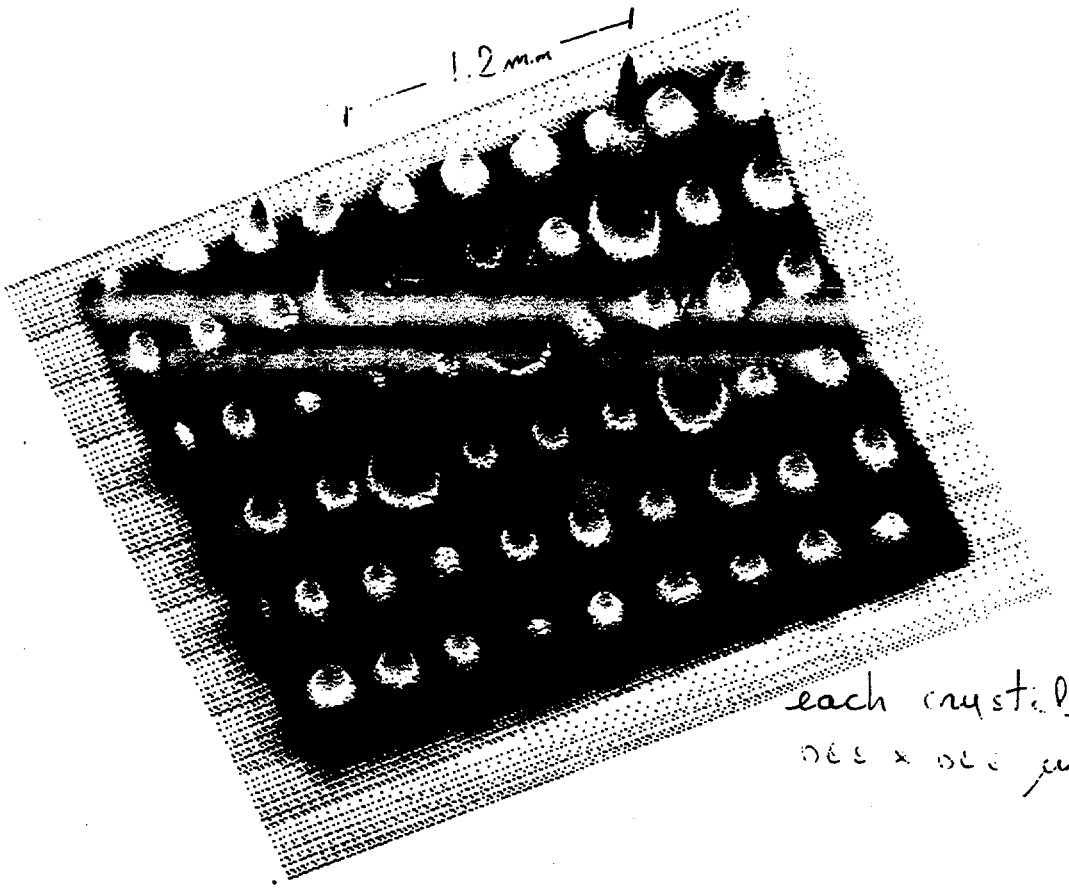
We have tried two basic configurations

- ISPA 1 : the photocathode is evaporated on a fibre optic window (glass)
  - adv.: high spatial resolution
  - drawback: poor spectral matching between YAP-emission spectrum and ISPA-window → low effective Q.E. → low energy resolution
- ISPA 3 : the photocathode is evaporated on Quartz
  - adv.: QE ≥ 25% → high energy res.
  - drawback: large cluster sizes

Space res $\propto \frac{\sigma}{\sqrt{N_{hit}}}$

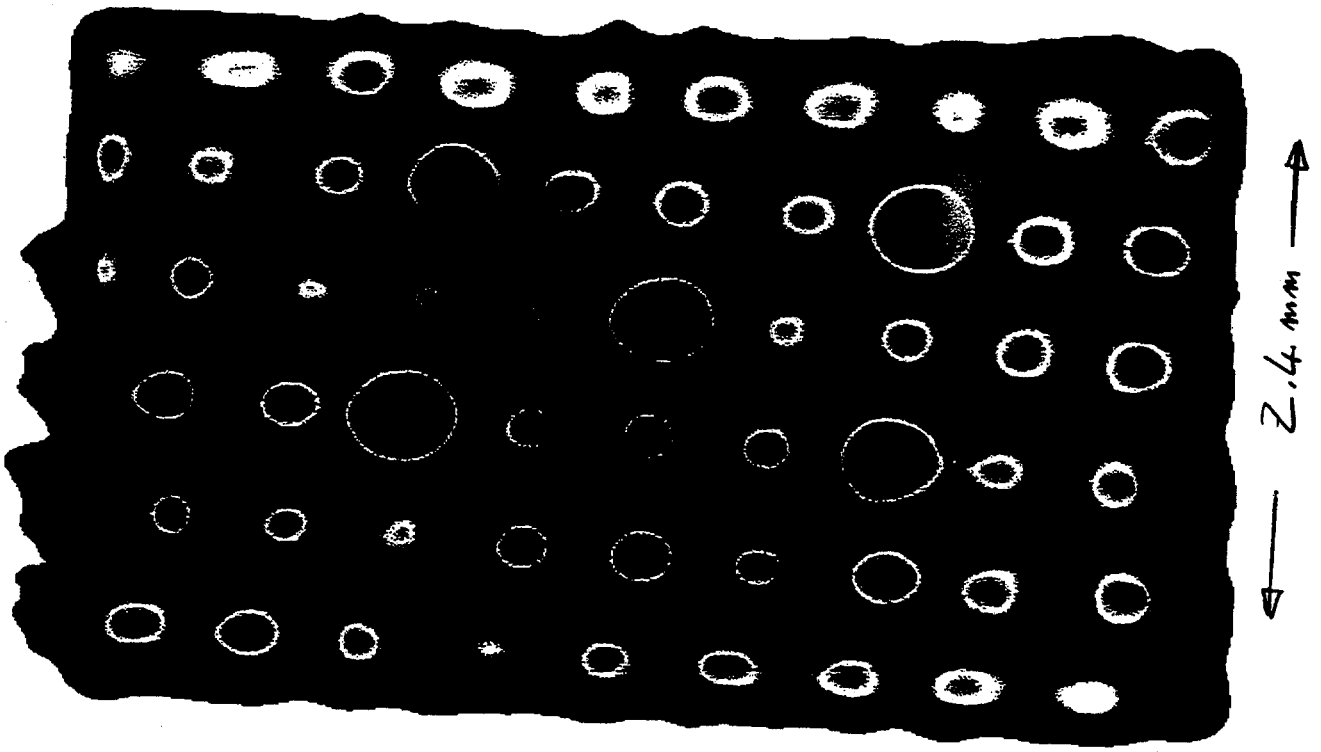
not to scale

3-D Plot

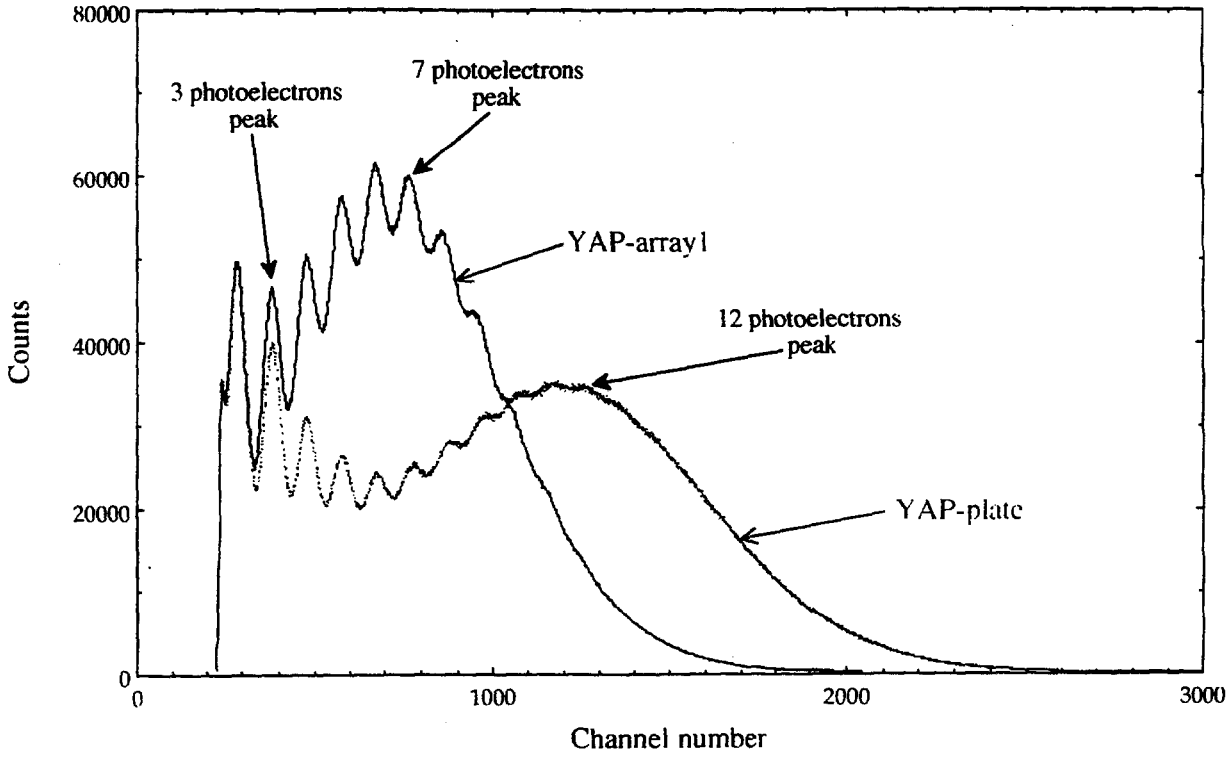


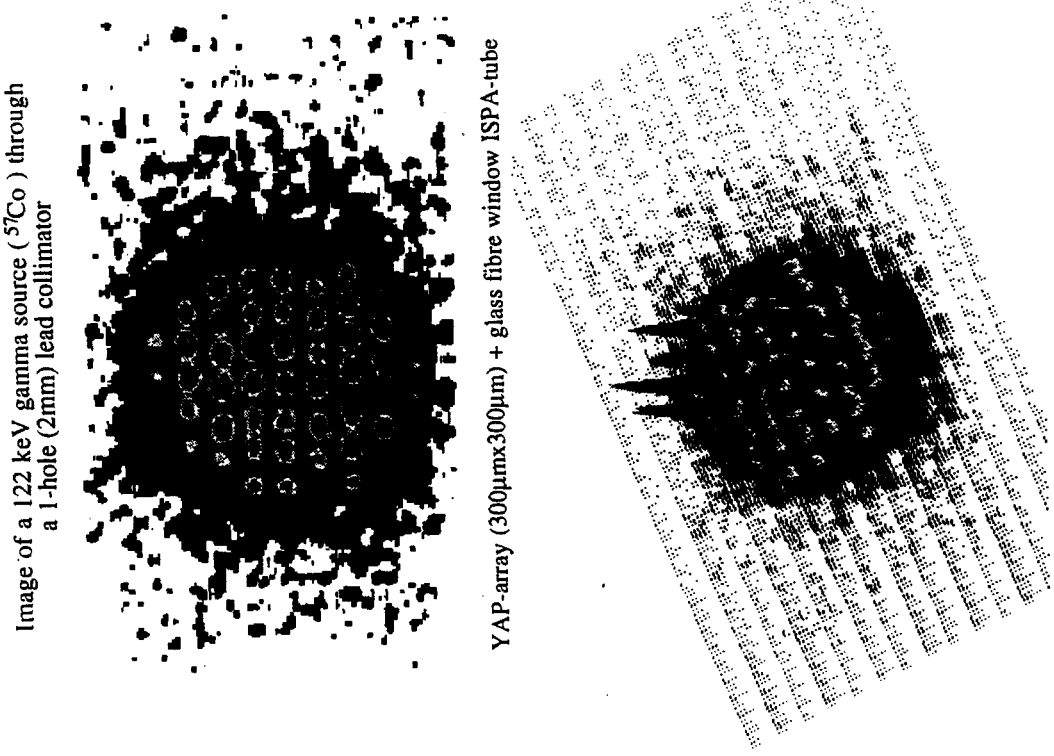
each crystal is
[illegible]

Gamma image of the collimator



Analog signal height distribution of 122 keV gammas detected by
a YAP crystal array or plate readout by an ISPA-tube with a glass fibre window





D.Pfeiffer et al.
CERN-INFN
Villa Olmo 96

Image of a 122 keV gamma source (^{57}Co) through a 2-holes (300µm) lead collimator

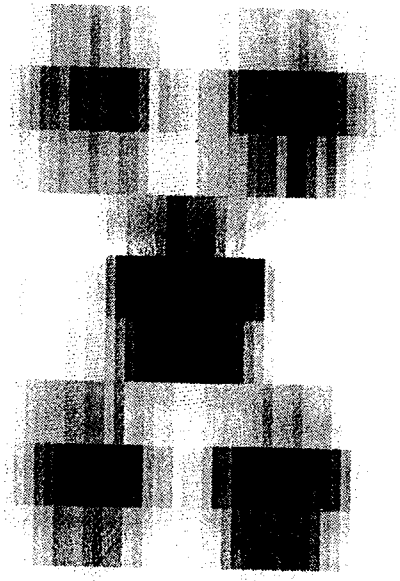
1.2 mm

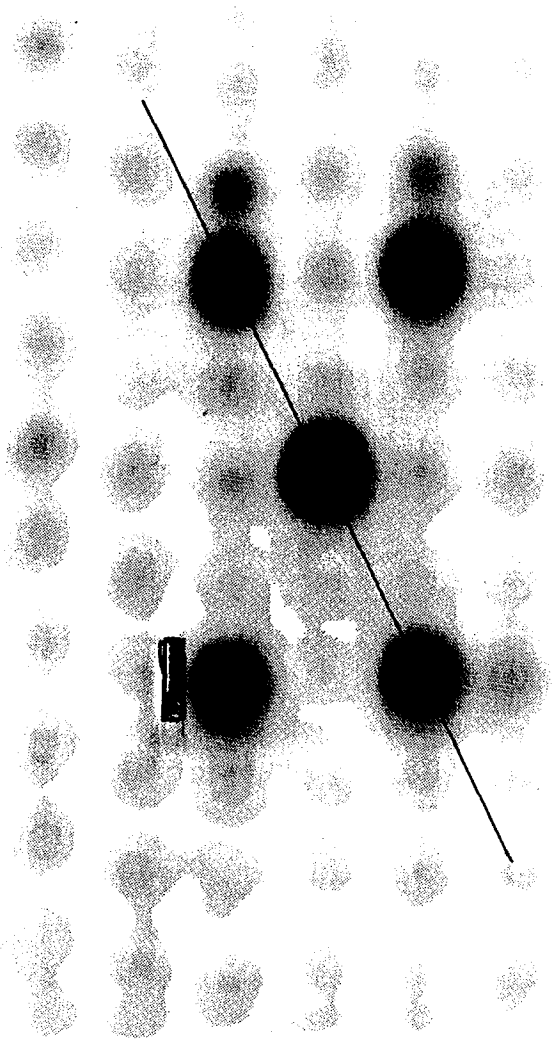
YAP-array (300µmx300µm) + Quartz window ISPA-tube

With the ISPA-tube,
two modes of acquisition are available:

- raw accumulation of events

- for each triggered event, a centre of gravity is calculated and then accumulated
    - higher resolutions $\left(\frac{\sigma}{\sqrt{N}}\right)$, but not applicable on line for very high trigger rates (do the analysis off line)





β - detection

for β – radiography of "in situ hybridization"

The active medium consists in either :

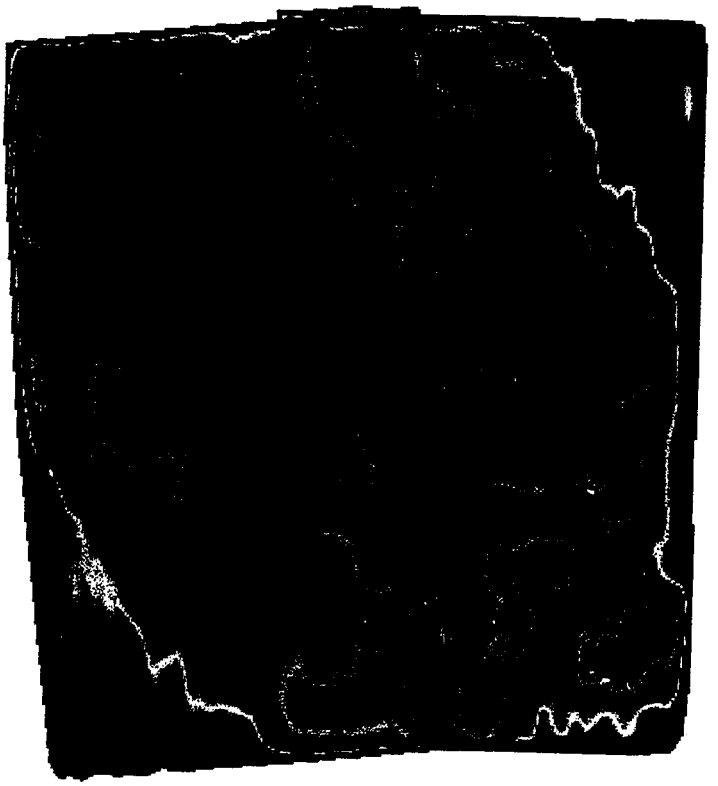
thin plastic scintillator sheets **(30 μm to 1 mm) or**

thin inorganic scintillators **(Si Y_2O_5)**

Application in Biology*: In Situ Hybridisation

- ^{35}S radioactive tracer in mouse cerebral trunk slices
- neurone calcium sensor protein

* In collaboration with M. Dubois Dauphin (CMU, Geneve)

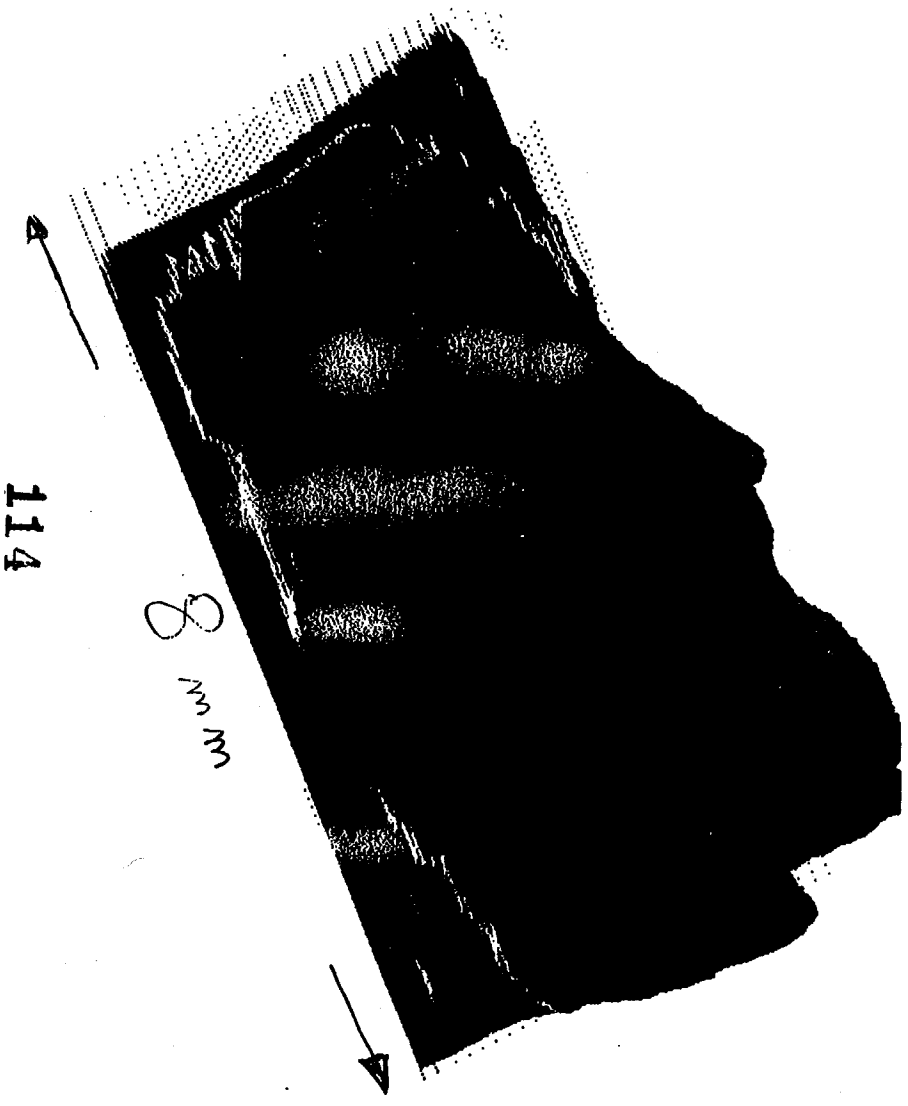


In situ Hybridization*
^{35}S

microslice of mouse brain

8 mm

*Work performed in coll. with Dr. M. DuBois-Dauphin at CMU-Geneve



FUTURE PLANS (Two years ago)

- ☞ new RD19 chips (LHC1) implementation is going on (see M. Campbell talk)
- ☞ increase active surface
  - larger photocathode
  - demagnification
  - several chips in one tube
- ☞ test of other scintillators and geometries
- ☞ new chip design better adapted to these applications
- ☞ evaporation of the PK directly on the crystal

Up to now, chips specifically developed for ionizing particle detection were used in the ISPA-tube. The results obtained are impressive. However, in order to:

- avoid complexity where not needed,
- scale up active surface,
- improve detection efficiencies for low energy photoelectrons and uniformity responce,
- decrease operating voltages,
- and minimize costs,

a specific chip is needed.

Its main features would be:

- Square pixel size (200 to 400 μm),
- Low threshold (~2000 el)
- Thresholds spread ~300 el at FWHM (or individually adjustable thresholds) } see Medipix (W. Snoeys talk)
- El. Noise ~500 el at FWHM
- Digital readout and logic part as for LHC1 chip
- Delay line tunable to 2÷3 μs
- Thinned detector unit with "no" dead layer
- Large detectors to bump-bond four electronic chips on } see ALICE

New ISPA Tube

For Single Photon Emission Tomography

Active Surface ~80 mm diameter

Spatial Resolution ~ 1 mm (FWHM)

Energy Resolution (at 140 keV) ~ 15 – 20 % (FWHM)

Counting Rates > 1 MHz / cm^2

80 mm diameter photocathode on quartz

Silicon chip surface 16 x 13 mm^2 (four times the LHC1 chip)

Electrostatic focussing Tube (demagnification ~5)

1 x 1 x 10 mm^3 YAP or CsI array

A similar tube is being developed as a candidate for the Rich-detector readout in LHC-b (see M. Campbell contribution)

Conclusions

ISPA - tubes as optoelectronic readout offer a powerful tool for a wide range of applications:

- for high - energy physics:

  charged particle trackers, active targets, Rich counters;

- for spectroscopy and astronomy:

  time-resolved position-sensitive photon-counting;

- for nuclear medicine

  hadron beam diagnostic, 2-D imaging, β- or γ- cameras;

- for biology:

  in-situ physiological processes diagnostic, etc.;

- for material analysis...

Recent Performance of Prototype Readout-Sensor Assemblies for ATLAS

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For the ATLAS Collaboration

Abstract

The past two years have seen the first use of fast (40 MHZ) pixel readout arrays in testbeam situations. Among other achievements, several LBL designed M72b readout chips were bonded to various sensors and successfully operated during the 1997 testbeam season. Results are presented here covering both the bench characterization and beam testing of various M72b detector/readout assemblies. In particular: threshold uniformity, timewalk, efficiency, resolution and Lorentz effects have been studied. Furthermore, first results from the current generation FE-B chips are also presented here.

1 Introduction

There are good reasons why pixels are the detector of choice for the innermost region of the ATLAS detector at the LHC. The small element size implies both low leakage current and low noise, making them intrinsically more radiation hard than strip detectors. In addition, the true 3-D information avoids tracking ambiguities. This is especially important at the LHC where each bunch crossing is expected to yield about 25 minimum bias events.

The design luminosity of the LHC is $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ with a bunch crossing rate of 40 MHz. Noise occupancy and timing constraints are driven by the desired track finding efficiency at this high luminosity. These constraints dictate that each hit in the detector must be correctly associated with a single bunch crossing. In other words, the cumulative time of charge formation, drift, pre-amplification and discrimination must vary by less than 25 ns for all signals of interest. The noise occupancy should be less than 10^{-5} hits per channel per bunch crossing. Furthermore, the physics goals of ATLAS require a point resolution of 12 μm in the rϕ direction and 100 μm in the z direction. Finally, ATLAS requires a pixel dead time of less than .5 μs.

These timing and occupancy requirements must be met by a pixel layer at an 11 cm radius for the entire life of the detector. At this radius, the lifetime dose is expected to be 200 KGy and 5×10^{14} 1 MeV n cm^{-2}. At the end of the detector life, the maximum attainable depletion depth is estimated to be about 100 μm at 200 Volts bias. Thus an in time threshold of about 2000 e^- would be required to keep losses from pulse height variations at a tolerable (below 1%) level. With this threshold, the noise occupancy requirement dictates that noise and threshold dispersion each be kept below about 200 e^-. These requirements can be relaxed if the detectors can be operated at higher bias voltages after irradiation.

The ATLAS pixel baseline calls for $50\mu m \times 300\mu m$ elements with binary read out. The detectors will be n^+ on n doped Silicon aiming at a thickness of 200-250 μm. The requirements and baseline decisions are explained in detail in [1].

Parallel prototyping efforts for the pixel readout electronics of the ATLAS detector have been underway in both Europe and the United States. For more details of the role of pixel detectors in the ATLAS experiment see [1], [2].

In the past two years an LBL-Wisconsin group has designed and tested two prototype versions of ATLAS pixel readout chips, M72b and FE-B. During 1997 the M72b chip was extensively tested both on the bench and in the H8 beamline at the CERN SPS. FE-B chips were received in mid-April 1998 and some very encouraging first results have been obtained.

2 The M72b Chip

The M72b chip represented a development phase of the ATLAS pixel project. It was intended as a test chip to prove the soundness of the readout architecture and the feasibility of meeting the electronics requirements. The front-end performance was not intended to meet all of the ATLAS requirements.

The M72b chip was fabricated in a .8 μm CMOS technology and supports an array of 12 columns of 64 50 μm $\times$ 536 μm pixels. The readout is column based. End of column (EOC) logic for trigger coincidence has been implemented. The coincidence is made using an externally generated 8 bit 40 MHz timestamp which is bussed to the end of column logic. If any pixels in a column fire, the timestamp is latched in an 8 bit by 8 deep buffer and the buffer address is written to a 3 bit latch locally at each pixel which fired.

Triggers are bussed to the EOC logic and a coincidence flags buffer elements for subsequent readout. If a trigger for a particular buffer element does not arrive when expected, the corresponding pixels must be actively reset and the buffer element cleared. Analog information is provided by integrating the discriminator output onto a storage capacitor. During readout, the stored charge for each hit pixel is multiplexed off chip and digitized. Test circuitry allows checking the pixel front end and the readout components of the chip independently.

2.1 M72b Bench Results

During the first six months of 1997 M72b arrays were extensively characterized on the bench at LBL. In general the digital performance was quite good. The analog performance was adequate, although not up to ATLAS requirements.

On the bench the M72b array-sensor assemblies performed with high efficiency and essentially no spurious hits down to thresholds of 3000 e^-. At these settings 400 e^- dispersion and 700 e^- noise were measured. Furthermore, the analog information was reasonably good. For any given pixel it was possible to measure the input charge to within approximately 1000 e^- up to input charges well over the MIP charge of 25000 e^-.

Fig. 1 shows some timewalk parameters from a chip that was not bonded to a sensor. The upper plot shows a per channel histogram of the time between the arrival of earliest hits seen on any pixel in the array and the average hit on each particular pixel when given a large (60000 e) input charge. The excellent (sub nanosecond) skew in timing across the array is largely attributable to the readout architecture. The lower plot is a per channel histogram of the input charge required for the timewalk to be under 25 and 50 ns. One can see from the bottom figure that the M72b array does not meet the ATLAS timewalk requirement.

Systematic studies of performance parameters revealed significant differences between odd and even columns with the odd columns behaving somewhat better. Eventually this problem was diagnosed as a layout flaw which allowed the ground reference for the discriminators in the even columns to float relative to that of the preamplifiers, resulting in modified threshold, noise and TOT behavior in these channels.

2.2 M72b Testbeam Results

The M72b array was characterized in a 180 GeV pion beam at the CERN SPS. M72b chips were bump bonded to both n^+ on n and n^+ on p detectors. The detectors were 300 μm thick and had a bricked geometry, i.e. alternate pixel rows were offset by one half pixel length. Data were taken at various bias voltages, V_{bias}, with the detector normal to the beam as well as with the detector rotated about the long pixel axis (ϕ) or the short pixel axis (θ). Runs were taken both field free and with a 1.5 T longitudinal magnetic field to simulate operation parallel to the beam in the ATLAS solenoid. A high resolution Silicon strip tracking telescope was also read out. All results presented here were obtained from events where a single high quality track, $\chi^2 < 1.5$ was found in the strip telescope. Track errors projected into the pixel plane were on the order of 3 μm.

Fig. 2 shows the detector efficiency as a function of V_{bias}. The efficiency was determined from the number of events in which a pixel cluster was found within 50 μm of the track intercept in the short pixel dimension. The trigger was asynchronous with the 40 MHz clock of the pixel electronics, so a TDC was available to indicate at what point in the 25 ns time bucket the trigger arrived. The open circle values were determined requiring the hit to have arrived either in same time bucket as the trigger or the next time bucket. This imposed a timewalk cut of anywhere from 25 ns to 50 ns depending on when the trigger arrived. The solid circle values were determined including hits from the next two time buckets as well. Finally, the star values were determined by eliminating events in which the trigger arrived less than 10 ns into a 25 ns time bucket. This was to eliminate events where large charges may have caused the pixel to fire before the early end of the accepted region. It can be seen that except for the case of very low V_{bias} and a tight timing window, the efficiency is between .98 and .99. With the TDC cut imposed the efficiencies are uniform at .99. Though the cause of the residual 1% missing hits is not fully understood, this result obtained with a 40 MHz chip having full EOC logic is encouraging. It should also be noted that the level of spurious hits was below the ATLAS requirement of 10^{-5} hits per channel per bunch crossing.

Fig. 3 shows the mean charge measured in a n^+ on p sensor as a function of bias voltage. In the events considered, there was exactly one cluster found in the pixel detector and this cluster was required to be within 50 μm of the

track intercept in the narrow pixel direction. The result of a fit to $\sqrt{V_{bias}}$ is shown on the figure. Unfortunately, most of the data from the n^+ on p sensors were taken at $V_{bias} = 40$ V, where the detector appears to be only about 75% depleted.

Fig. 4 shows the resolution measured along the short axis of the pixels with various levels of readout information as a function of ϕ. The cluster position was estimated by a simple charge centroid. As ϕ is increased, the number of clusters which span more than one row increases. We see that the best resolution comes at 10° when two pixels fire much, but not all, of the time.

Fig. 5 shows the effects of bricking. As with the short axis, the cluster position was estimated by a simple charge centroid. As ϕ is increased, the number of clusters which span more than one row increases. The added information this yields in a bricked detector, even with this simple position estimate, is exhibited in the strong ϕ dependence of the residual distribution. In confirmation of this, it was found that for a given cluster width the residual was nearly independent of ϕ.

Finally Fig. 6 shows the mean number of rows spanned by a cluster as a function of ϕ with and without the 1.5 T field. A Lorentz drift angle of approximately 9° can be estimated from the figure. A monte carlo study is underway to better understand the charge collection and should help interpret this behavior.

3 FE-B Chip

The FE-B effort, as with the M72b chip, uses a timestamp to make the trigger coincidence. Although the ATLAS baseline calls for binary readout, FE-B prototypes provide charge information via a time over threshold (TOT) measurement. In this generation the timestamps are bussed directly to the pixels, latched on the rising and falling edges of the discriminator and then written to end of column buffers. Buffering is provide for up to 20 hits from 16 different triggers. The M72b chip could handle events with an arbitrarily large number of hit pixels. Those pixels were then dead until read off of the chip. The FE-B chip can not store more than 20 hits per column pair at a time, however, the pixel deadtime is much shorter, being roughly equal to the return to baseline of the pre-amplifier. At 40 MHz, a 5 bit TOT measurement

would give a pixel deadtime of roughly 800 ns. Another feature of FE-B is a dual level discriminator. The low discriminator determines the hit timing as well as the time over threshold, while the high discriminator validates the hit. The aim of this configuration is to satisfy the timewalk requirement within the power budget and without introducing excess crosstalk. Furthermore, each pixel contains a three bit tuning DAC which acts as a vernier adjustment for the threshold in that pixel. These tuning DACs can be individually set so as to minimize the threshold dispersion. For a detailed discussion of the FE-B pre-amplifier and discriminator configuration see [3].

3.1 FE-B Bench Results

Since the FE-B wafers' arrival at LBL on April 15 a wafer probe station has been commissioned and wafer probing is underway. Individual chips have also been probed on single chip support cards.

The results have been extremely positive. Aside from a bug in the priority scan that causes many hits from columns 11-18 to be lost, the chips have been nominal and the yield has been extraordinary. On the first wafer probed, 81 of 85 chips passed all tests.

So far, FE-B arrays without detectors have been operated at a 5000 e^- threshold setting with 450 e^- dispersion without use of the tuning DACs and less than 70 e^- noise. After tuning a 3000 e^- threshold with 100 e^- dispersion was achieved.

3.2 FE-B plans

Currently work is underway to produce module controller chips, MCCs, to be used in fabricating pixel modules. The modules will be composed of 16 front end chips with 18 columns of 160 pixels each mounted on a single detector substrate and read out through a MCC. The division of functionality between the two chips is close to that of the final system. The modules will first be fabricated in rad-soft technologies. After the successful completion and testing of the rad-soft versions, rad-hard submissions will follow.

4 Conclusions

Silicon pixel detectors offer an answer to many of the challenges of running at the LHC, but come with many challenges of their own. Though the first ATLAS prototypes were not intended to meet all of the requirements of this harsh environment, results obtained with them are encouraging. Despite a 2005 LHC turn on date, detector production, testing, installation and commissioning time scales make the immediate schedule tight. The second round of prototypes have yielded some very positive first results.

References

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[2] G. Gagliardi, these proceedings.

[3] F. Pengg, Proc. 1997 IEEE Nuclear Science Symposium, Albuquerque, Nov 9-15, 1997, to be published in TNS.

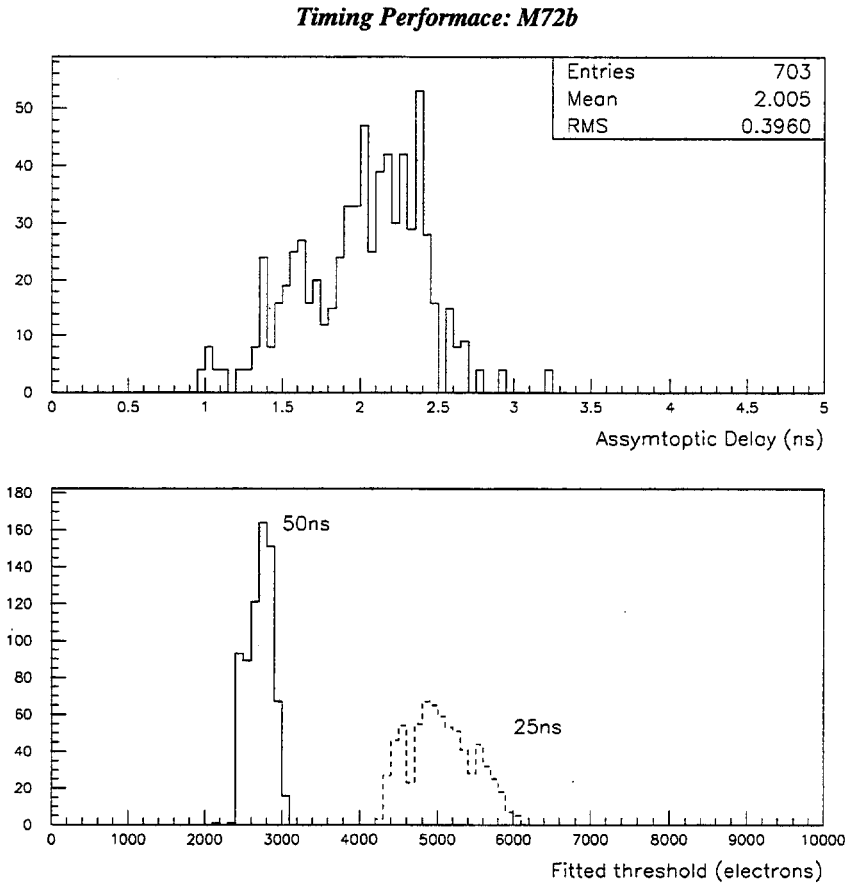


Figure 1: top) Timing skew across the M72b array. bottom) Threshold in electrons for hits to arrive within given delays.

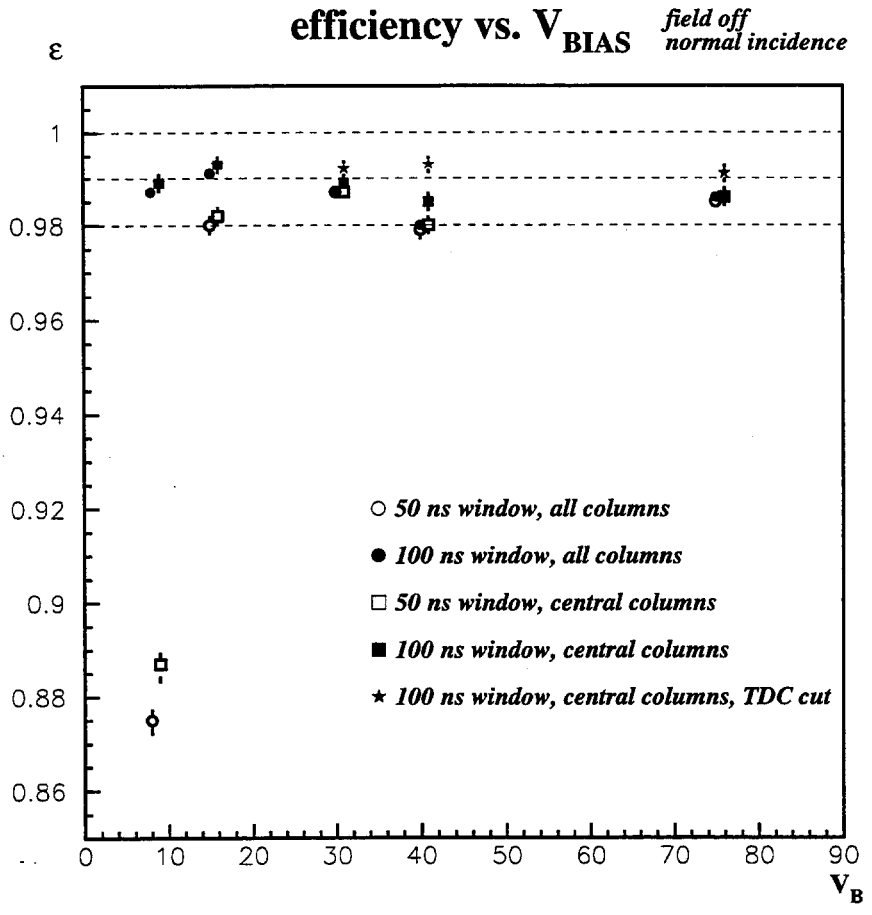


Figure 2: Efficiency as a function of bias voltage at normal incidence for an n^+ on p-bulk detector operated partially depleted. The various data sets are described in the text.

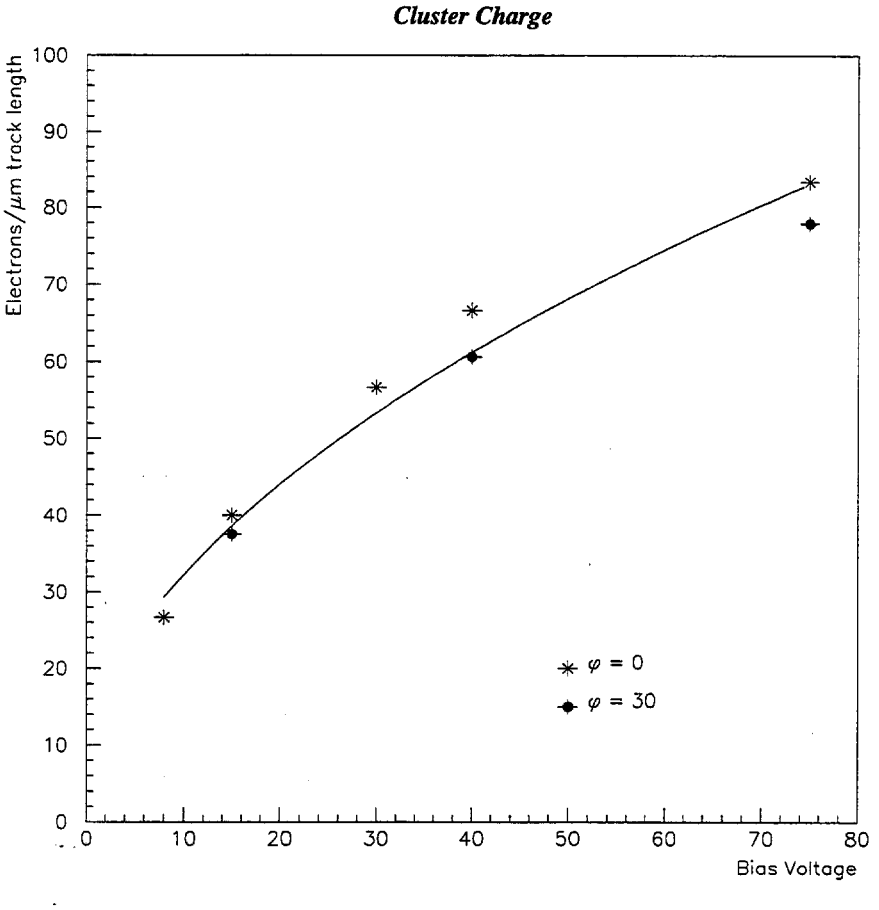


Figure 3: Mean charge deposited in the n^+ on p-bulk detector per track length as a function of the bias voltage.

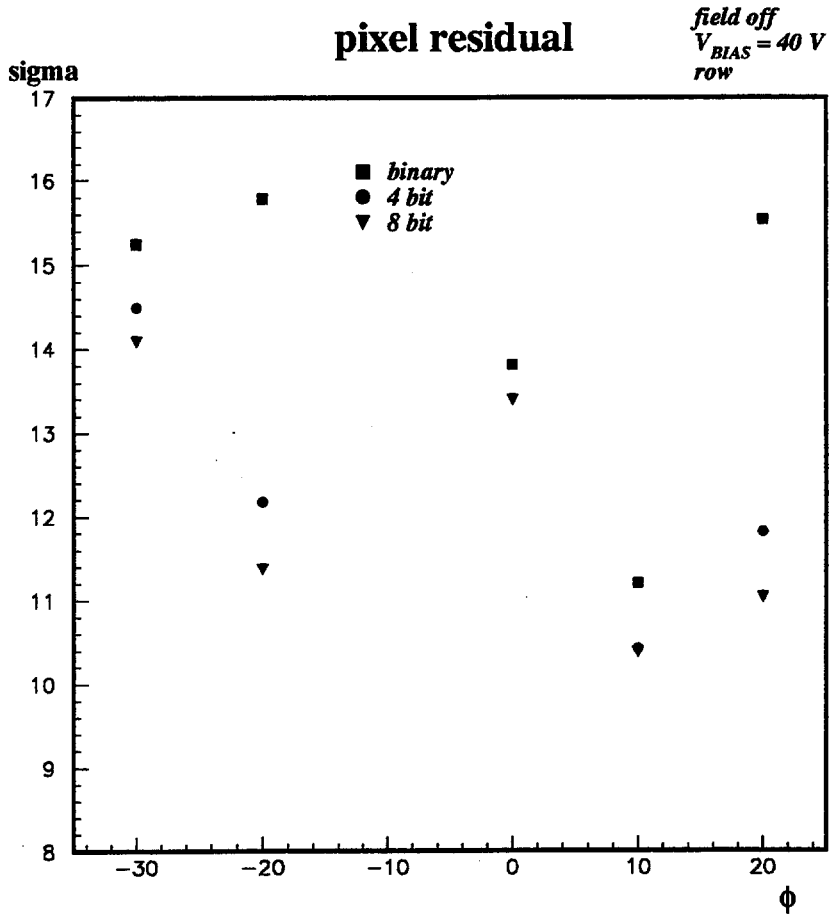


Figure 4: RMS of the residual distribution between the track projection and the pixel cluster location in the short pixel dimension as a function of ϕ.

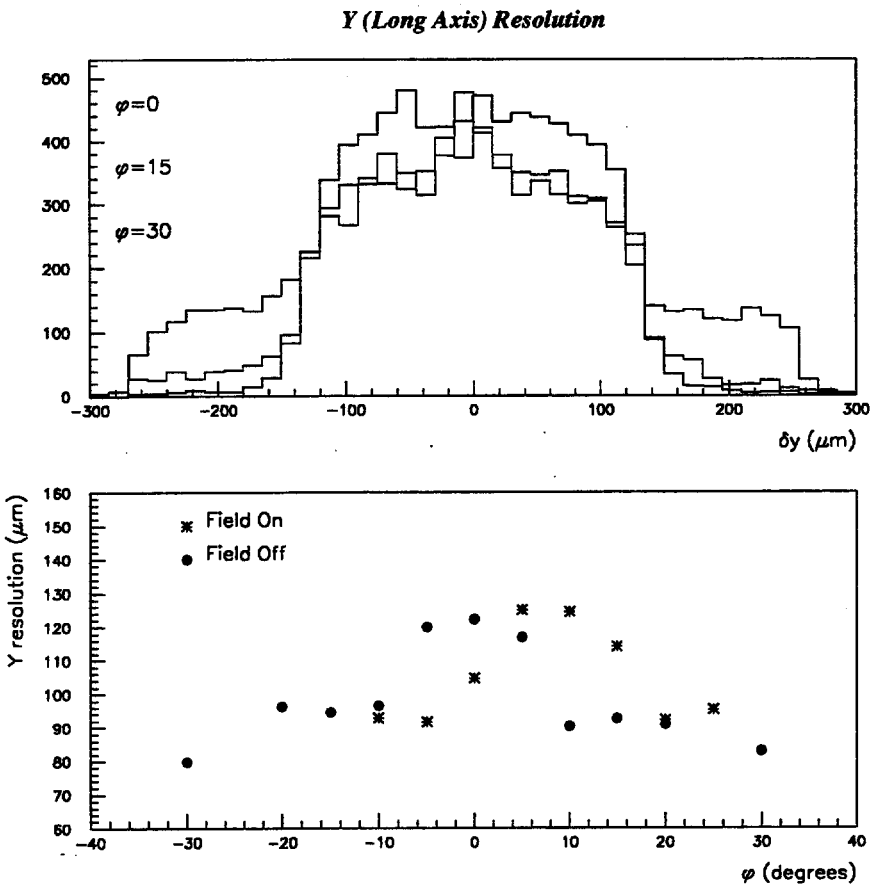


Figure 5: top) Histograms of residuals in the long pixel dimension for various ϕ. bottom) RMS of the residual distribution between the track projection and the pixel cluster in the long pixel dimension as a function of ϕ.

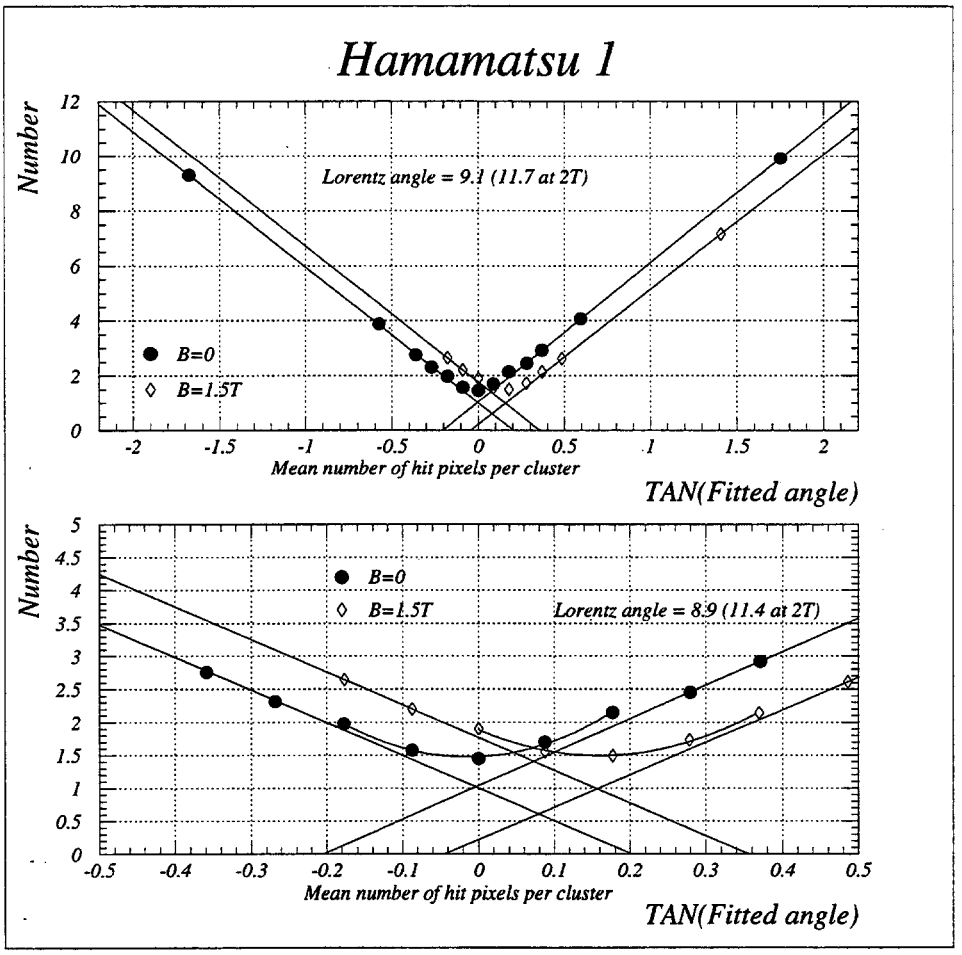


Figure 6: Mean number of rows spanned by a cluster as a function of ϕ with and without the magnetic field.

US ATLAS Pixel Electronics

K. Einsweiler, LBNL

LBL/Wisconsin electronics team: E. Charles, A. Ciocio, K. Dao, D. Fasching, A. Joshi, S. Kleinfelder, L. Luo, R. Marchesini, O. Milgrome, F. Pengg, J. Richardson, G. Zizka

ATLAS Pixel Electronics:

- Electronics requirements for ATLAS
- Electronics design effort:
  - → "Proof-of-Principle" phase (essentially complete)
  - → Realistic prototyping phase (now in testing phase)
  - → Production phase

Proof-of-Principle phase:

- Chips fabricated
- Lab and testbeam results

Realistic prototyping phase:

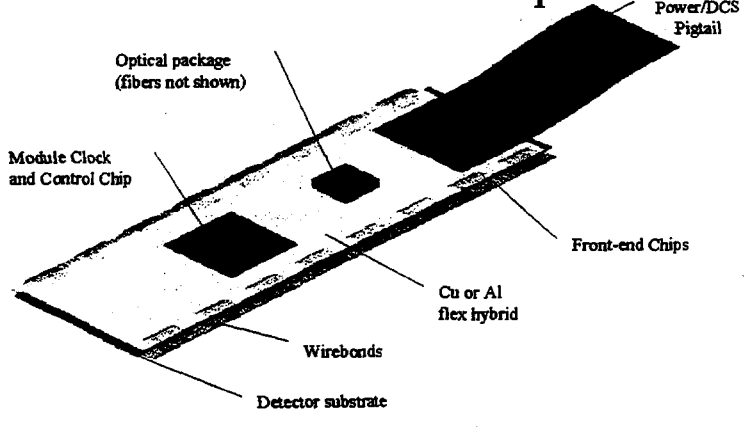
- ATLAS1 Chipset: design overview
- Design details and first results from FE-B chip

Overview of ATLAS Pixel Tracker

Basic Component:

- Modules which are placed on a mechanical support and cooling structure in "chips down" configuration, with detector substrate smaller than electronics:
  - → Silicon detectors (one per module), with active size roughly 16.4 x 60.4 mm
  - → Electronics chips bump-bonded to detectors (16 FE chips and 1 Controller chip per module)
  - → Hybrid interconnect that connects front-end chips to controller chip and services

Disk Module Concept



Pixel Electronics Requirements for ATLAS

High overall efficiency is necessary:

- Pixel layers are complex, costly, and contain lots of material.
- Inefficiency sources include dead/inefficient regions, timewalk performance, electronics deadtime, masked or dead electronics channels, and high thresholds.
- Goal is for each of these to contribute less than 1% to the global hit inefficiency.

Maximum power budget is 0.6 W/cm^2, or 5.5 W/module:

- This corresponds to 250 mW/front-end chip and ≈40 μW/pixel front-end.
- It allows 300 mW for module control, and 300 mW for detector leakage.
- It allows up to ≈900 mW for power transmission and data transmission.

Radiation tolerance is at least 30 MRad, or 100 MRad for inner layer over full lifetime (silicon detectors would die).

Geometry of pixel and front-end chip:

- Pixel geometry determined by point resolution and feasibility ≈ 50μ x 300μ.
- Chip geometry determined by radhard yield, suggests die should be < 80 mm^2
- Goal: 24 column x 160 pixel matrix with ≈2.5 mm "deadspace" for peripheral logic.

Front-end requirements:

- Minimum silicon signal after 10^{15} fluence is ≈6 Ke. Efficient detection requires a threshold of about 2 Ke.
- Operating at this threshold requires a noise of less than ≈200 e, and a threshold dispersion of no more than ≈200 e.
- The timewalk should be small enough to allow 40 MHz beam-crossing association down to roughly the minimum threshold.
- The input capacitive load is expected to be about 200 fF.
- The DC-coupled preamplifier should handle leakage currents up to 50 nA/pixel.
- The noise occupancy should be below 10^{-6}/pixel/crossing.
- The crosstalk ratio (threshold/adjacent signal to fire neighbors) should be <5-10%

Readout architecture requirements:

- Unique beam-crossing association at 40 MHz.
- Store information for 2.5 μs L1 latency and handle 100 KHz accept/readout rate.
- Operation at pixel occupancies as high as 5x10^{-4}/pixel/crossing with deadtime <1%, implying no more than ≈500 ns deadtime per hit.
- Adequate buffering in perpheral logic to prevent significant hit loss, even for large local occupancy fluctuations (e.g. inside of jets where chip occupancy x 10-20).

The LBL Matrix (M72b)

The front-end design:

- The front-end design uses a fast high-gain preamplifier with an unusual "leakage subtraction" circuit, and provides linear TOT up to very large charges.
- A simple discriminator follows, giving reasonable threshold dispersion (250e), but only fair timewalk (50 ns required for pulses near threshold). The disriminator output is integrated on a capacitor to provide analog TOT information.

The readout architecture:

- Pixel address and charge information is stored in the array in a "content-addressable memory" structure which can retain 8 simultaneous events.
- Timing information is stored in the peripheral logic for each event on a per-column basis using an 8-bit Grey code timestamp and a 2-level buffering scheme to store 8 events prior to trigger coincidences and 4 events pending readout.
- A 2D sparse-scan readout system allows transfer of this information off-chip at up to 10 MHz. Only hits above threshold for triggered crossings are read out, and each hit contains the pixel address and timestamp, plus the analog charge information.

Pixel Electronics Development Program

ATLAS requirements go far beyond existing pixel systems

- "proof-of-principle" prototyping was carried out to explore different concepts and see if 40 MHz concurrent operation at low threshold was achievable.
- These first chips have achieved many of the ATLAS requirements.

Two major efforts were carried out inside ATLAS:

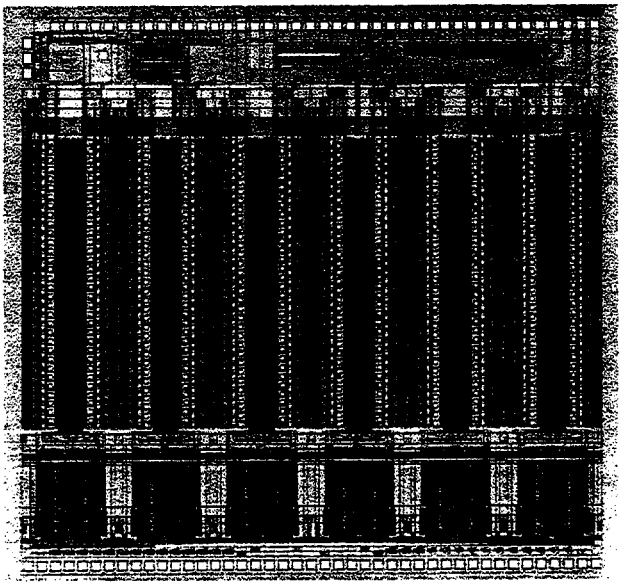
- Bonn/CPPM matrix: a 12x63 pixel array with 50μ x 436μ pixels and no peripheral logic, providing digital TOT information, fabricated using AMS 0.8μ BiCMOS process (see talk of T. Kuhl).
- LBL matrix: a 12x64 pixel array with 50μ x 536μ pixels and complete peripheral logic, providing analog readout of TOT information, fabricated using HP 0.8μ CMOS process (see talk of E. Charles).
- Extensive lab characterization and beam testing has been performed on both.

Now have moved to realistic ATLAS prototypes:

- Learned many lessons from prototypes and subsequent development work.
- Incorporate complete set of functional blocks required for module construction.
- ATLAS1 chipset includes 2 front-end chips and 1 module controller chip initially radsoft, but targeted for radhard.

Chip Layout:

- Pixel input pads use staggered geometry (100μ bump separation) and inputs are in center of pixel to support bumping to "bricked" detector geometry
- Peripheral logic includes 2 levels of FIFO buffering per column and sparse scan.
- Digital readout logic is on bottom, analog biassing and test points on top



Summary of Tests (see talk of E. Charles for more plots):

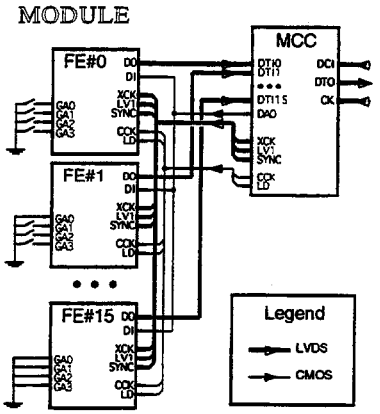
- Initial tests were performed with n^+ on p-bulk detectors fabricated at LBLn abd bump-bonded by Rockwell (now Boeing). They provide partially depleted operation, with only single-sided processing.
- Electronics was operated at a threshold of ≈ 4 Ke.
- Extensive testbeam data was aqcuired at CERN in Apr. 97, showing excellent bump-bonding and efficient operation down to depletion depths of ≈ 100μ.
- A second set of tests was performed with baseline n^+ on n-bulk detectors, fabricated by Hamamatsu.
- Four detectors were tested in the CERN testbeam in Sept. 97, and operated efficiently with V(depletion) ≈ 65 V and low bias currents.
- In collaboration with the RD-42 diamond R&D effort, we have fabricated an assembly using a piece of the 600μ D73 diamond detector. It has been bump-bonded by Boeing using their Indium bump-bonding technology. First results will be presented at this meeting by W. Trischuk.

The ATLAS1 Chipset: Definition and Development

Address ATLAS requirements with definition of new chipset

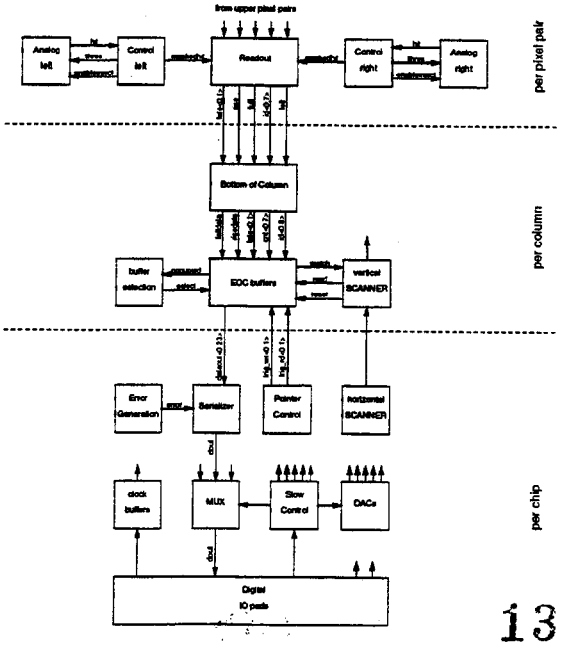
Based on system design concept with novel features:

- All control of the chips involved uses serial command interfaces
- Module interface is three wires: DataIn, DataOut, and Clock
- All fast digital activity uses LVDS drivers/receivers with ≈ ±300 mV swings
- Data (both event and configuration) is output over a 40 MHz serial link
- Module Controller Chip (MCC) drives signals to 16 Front-end chips, collects return data and build events using a star topology for bandwidth and redundancy.



Front-end chip design proceeded in two parallel directions:

- One effort is targeted for the DMILL radhard process, and follows closely the successes of the BP51 chip development (FE-A).
- The other effort is targeted for the Honeywell radhard process, and is based on new developments in the front-end and architecture areas (FE-B).



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Common features of two front-end chips:

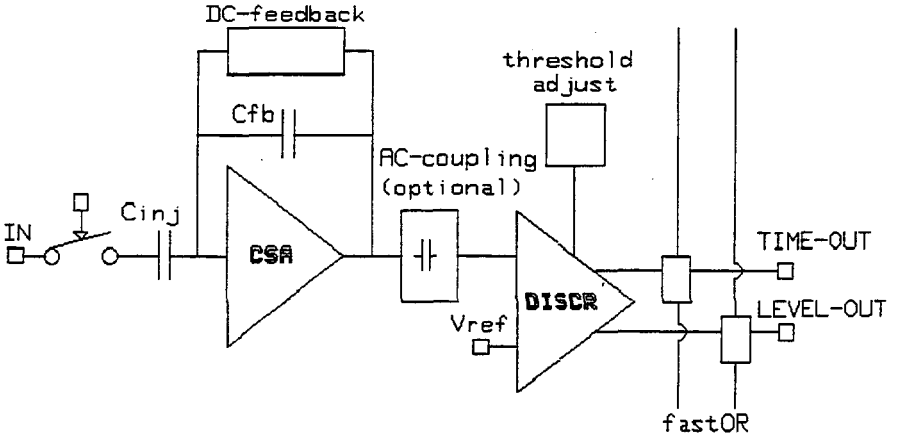
- Two FE designs are "pin-compatible", meaning pin assignments are identical, and they can be operated with the same MCC and test boards, although internal registers and their meanings are somewhat different.
- The geometry is 18 columns of 160 50μ x 400μ pixels with 50μ pitch bump pads. The die size is 7.2 x 10.8 mm, with 2.8 mm for all peripheral logic.
- Front-end biassing is controlled by an internal current reference and up to 8 current-mode 8-bit DACs, with bias points brought out for decoupling/reference.
- The readout architecture is column-pair based, meaning that two adjacent columns share a readout structure and enter a common EOC buffer block.
- The data is transferred from the pixels to the EOC buffers as soon as it is ready to minimize the total deadtime close to that required for the front-end alone.
- A 4-bit trigger number field is used to store up to 16 triggers pending readout.
- The protocol is "data push" where each FE chip receiving a L1 Trigger produces at least one data word. Data is sent out in the order triggers are received.
- The data format includes a 1-bit header and 25 data bits: 4-bit L1, 13-bit Row/ Column, and 8-bit TOT, for each hit.
- A serial command processor with simple command format is used to read/write all internal registers. A MUX determines whether event data or register data is returned over the serial link.

Front-End B (HP/Honeywell version)

Front-end design:

- Basic design uses a fast, high-gain DC-coupled preamplifier, followed by an AC-coupled slower differential amplifier, followed by a dual-threshold discriminator block:

BLOCK DIAGRAM OF THE ANALOG FRONTEND



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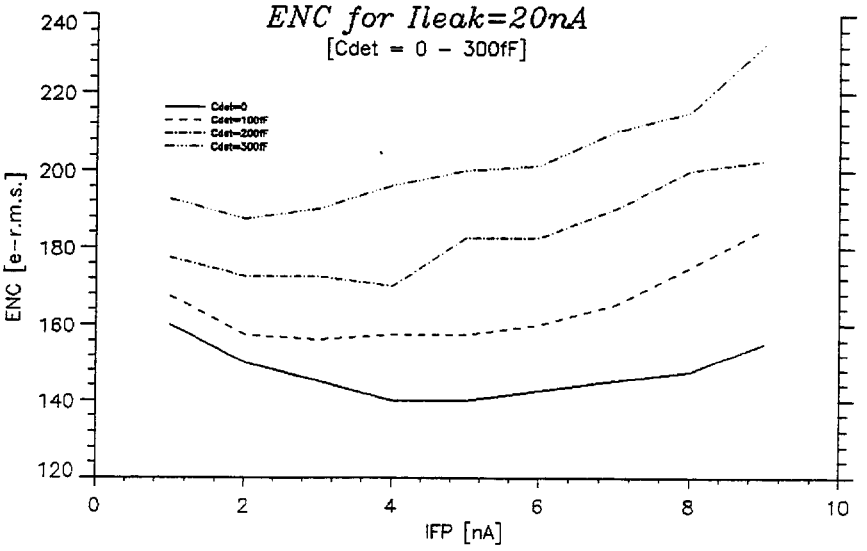
Preamplifier design details:

- Preamp uses direct cascode for lower input impedance, and has a peaking time of about 30 ns.
- Feedback circuit is based on design of CPPM (L. Blanquart), and uses C(feedback) = 3.5 fF to avoid saturation. This feedback scheme has a very high tolerance for leakage current.



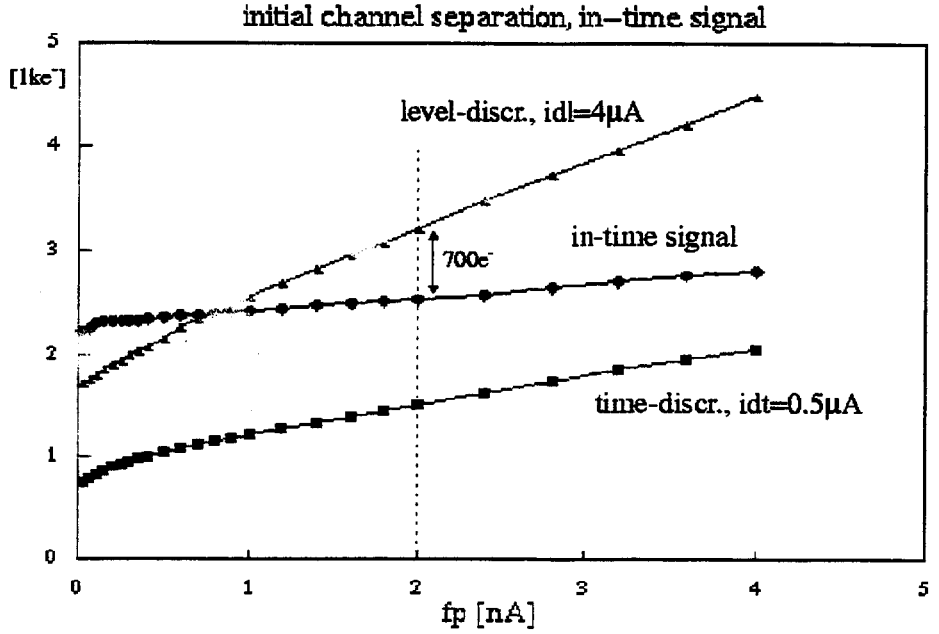
Differential Amplifier coupling stage design details:

- AC coupling uses novel technique to get best possible return to baseline.
- This is followed by a relatively slow (80 ns) but high gain differential amplifier to reduce crosstalk while retaining timewalk performance. The crosstalk suppression arises because the cross-coupled signal from the neighboring channels is faster than the primary signal from the detector. This approach offers reduced power consumption but suffers from greater sensitivity to the preamplifier shaping behavior.
- Threshold control is provided by adjustment of the differential amplifier baseline (coarse control) and by adjustment of the individual discriminator biases (fine control).
- A 3-bit in-pixel DAC is also provided for threshold tuning of individual pixels. The step size of the DAC is adjustable globally.

Dual Threshold Discriminator design details:

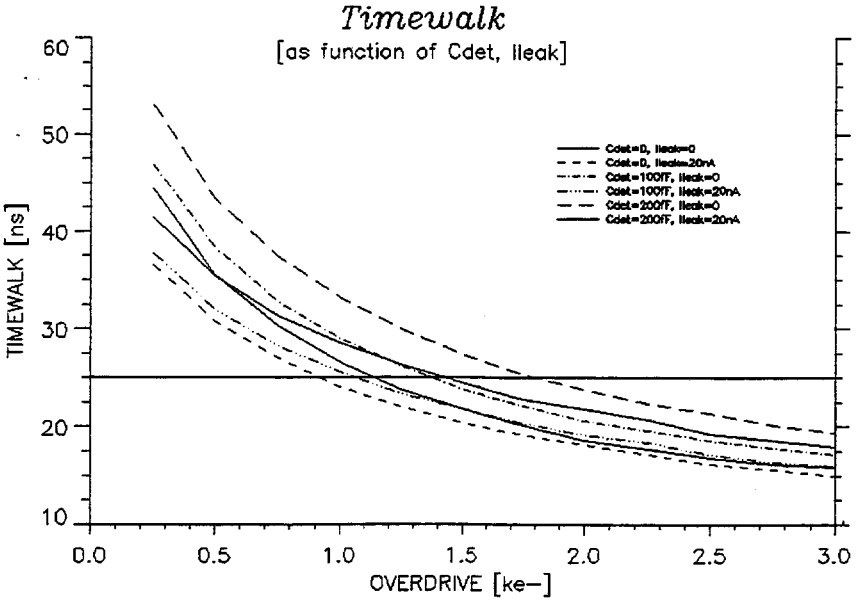
- A dual-threshold discriminator scheme is used to eliminate out-of-time hits, and provide flexibility by decoupling the low threshold required for optimal timewalk from the higher threshold needed for optimal crosstalk and low noise occupancy.

- The idea is that the high threshold is set to optimize noise occupancy and efficiency, and then the lower threshold is set so that its "in-time" threshold is lower than the high threshold, thereby eliminating out-of-time hits.:



Prototype results:

- A series of prototype test chips have been used to evaluate this design (and many variations). The present performance indicates a timewalk of 25 ns is achieved with an overdrive of about 1500e for a 35 µW power budget for the front-end:



- A threshold dispersion of about 300e RMS (before tuning) is achieved.

Command decoder and control features:

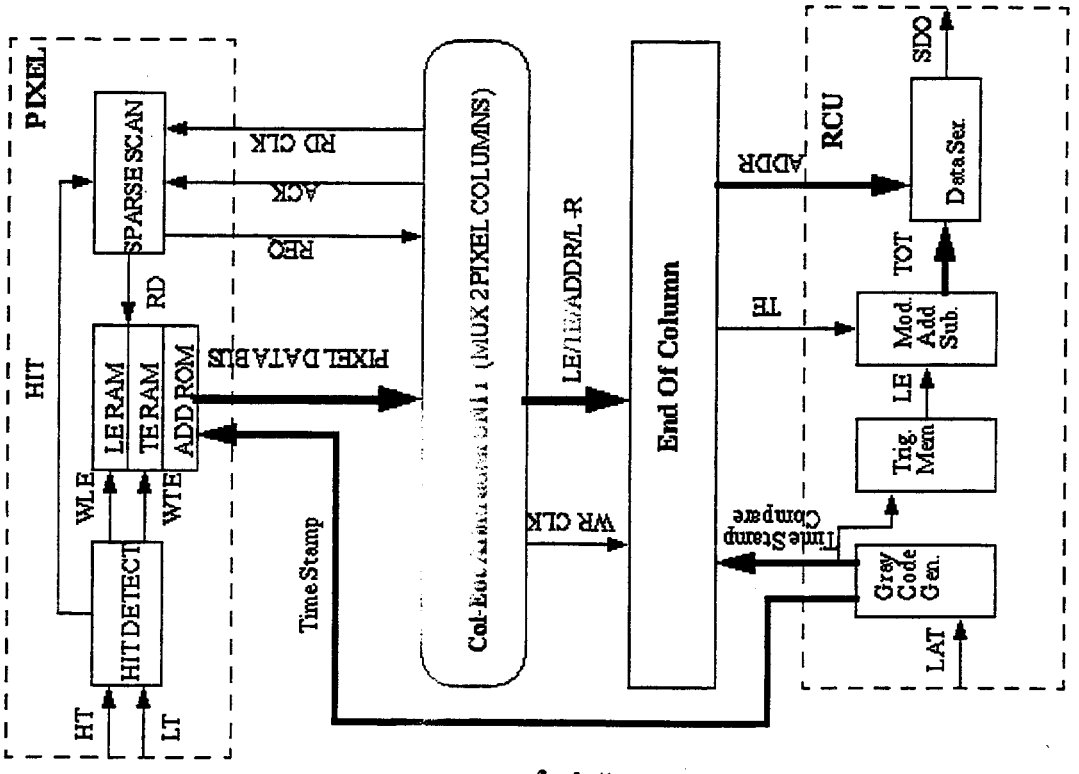
- The chip supports a simple serial protocol for writing and reading the internal registers. Presently, this runs at 1/8 of the full clock speed (5 MHz).
- Command Register includes:
  - → Single Discriminator Mode, FastOR Enable, Preamp Buffer Enable, Analog Injection Enable, Digital Injection Enable
- DAC Register for controlling 8 8-bit current-mode DACs which control biasing for:
  - → Preamp bias, Feedback, AC-coupling bias, Diffamp bias, Diffamp baseline, Dual-discriminator biasses, and step size of 3-bit TDAC. Value of 0 disconnects internal current source to allow external setting.
- Global Register includes:
  - → L1 latency control, DO MUX, Column Clock speed, TDAC values.
- Pixel Register includes:
  - → Select bit for charge injection control, Mask bit for readout control, 3-bit TDAC value.
- Hit Injection:
  - → Can occur digitally at input to readout logic, with pulse width given by external Strobe, analog via an internal VCal "chopper" in the chip periphery, or analog via an external chopper pulsing VCal.
- Monitoring:
  - → Provide two FastOR differential outputs from array, with participation controlled by Readout Mask
  - → Provide single buffered Preamplifier Output.
  - → Provide access to current reference used by internal DACs. Value can be set by external voltage.

Readout architecture:

- Individual pixels contain leading-edge and trailing-edge latches to record a 7-bit Grey code timestamp which associates the hit with a 40 MHz beam crossing.
- A hit is initiated by the leading edge of the low-threshold input. The TOT is determined by the trailing edge of the low-threshold input. The hit must be validated by the presence of a high-threshold input during the period in which the low-threshold discriminator is also turned on, otherwise the hit is reset.
- Pixels operate independently, and transfer their data to the EOC buffers immediately after the trailing edge occurs, over a shared (arbitrated) bus which services the two columns in a pair. The arbitration logic lives in the "bottom-of-column" region between the column and the end-of-column buffers.
- Hits are drained out of the column pair by two parallel ripple-through sparse scan circuits. These circuits use a look-ahead mechanism (10 groups of 16 pixels are scanned in parallel) to achieve a ripple-down time of about 25 ns in a 160 pixel column. This mechanism ensures that the "highest valid hit" in each column is presented for readout to the bottom-of-column arbitration circuitry. A column clock is used to synchronize this activity and eliminate metastable states.
- The EOC buffer block for a column pair contains 20 buffers to store hit information. The leading-edge timestamp, the trailing-edge timestamp, the 9-bit address, and the 4-bit trigger number are stored. Three status FF implement a simple state machine. The states are: Hit, Triggered, Readout Pending.

- The L1 latency is generated by two "offset" Grey counters, one of which supplies the pixel latches (distributed to 2880 pixels !) and one of which supplies the 7-bit comparators in each EOC buffer location. The latency is programmable from 1 to 128 crossings.
- The readout controller circuit keeps track of up to 16 triggers in a FIFO, storing the leading-edge timestamp, and the buffer overflow status bit.
- The overflow flag is a wire-OR of all EOC buffer full status lines, stretched by one L1 latency (the longest period over which an overflow can affect an event). It is transmitted in the End-of-Event word.
- A TOT subtractor unit combines the leading-edge and trailing-edge information, correcting for the latency, and provides the TOT as an 8-bit count.
- Hits are transmitted serially in individual 26-bit packets (1 header bit, 4 trigger bits, 8 row bits, 5 column bits, 8 TOT bits). Significant redundancy allows detection of errors, but no correction is possible. Illegal row numbers (224 and 240) are used to indicate End-of-Event words.
- The data serializer is pipelined to ensure gap-free transmission of the hit packets. A tenth "phantom" column supplies the End-of-Event word in all cases. The generation of an EOE word for every trigger accept is required to simplify event building in the MCC.

Simplified Block Diagram of Readout Architecture:



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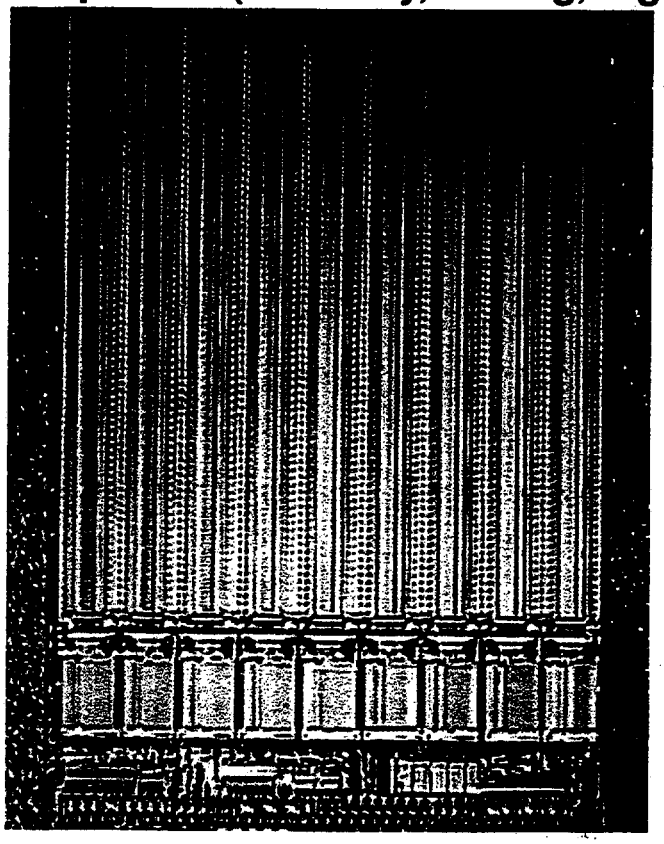
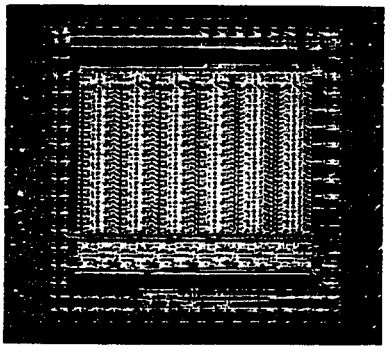
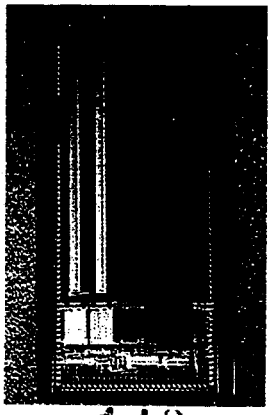
Status (see plots in talk of E. Charles):

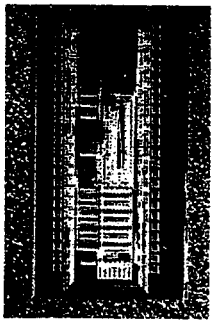
- The complete pixel array was submitted to MOSIS/HP on Feb. 23 for fabrication. The array contains 840K transistors, with about 250 per pixel in 50μ x 350μ.
- The reticle included:
  - → Two pixel arrays
  - → Analog test chip with 6 columns of front-ends, including biassing and DAC plus current reference circuitry. Many internal signals available, plus can apply capacitive loads and inject leakage currents.
  - → Digital test chip with 2 column pairs and 24 direct injection points to allow parallel load studies of the readout. The complete peripheral logic is included. Many internal nodes are brought out.
  - → A command decoder and I/O driver/receiver test chip.
- The wafers returned on Apr. 17, and die have been tested. Several minor errors were found, but chips perform largely as expected. Power is: DVdd = 50 mW, AVdd+AVcc = 170 mW of which 40 mW is FastOR buffers and 120 mW is pixels.
- Only serious error is a timing problem in the horizontal sparse scan of the EOC buffer blocks, which causes the readout of the last 8 of 18 columns to be unreliable. This means that only 1600 channels behave perfectly on each chip.
- A first wafer was probed earlier this week, with a yield of 81/85 good die (95%), and all 129,600 expected good channels operated correctly under digital injection. Operation at 40 MHz on the probe station, with analog charge injection has been quite successful, with noise levels of about 100e observed. Wafers are now out for bump deposition and flip-chipping, will go to testbeam in June.

Die photos (full array, analog, digital, and command chips):









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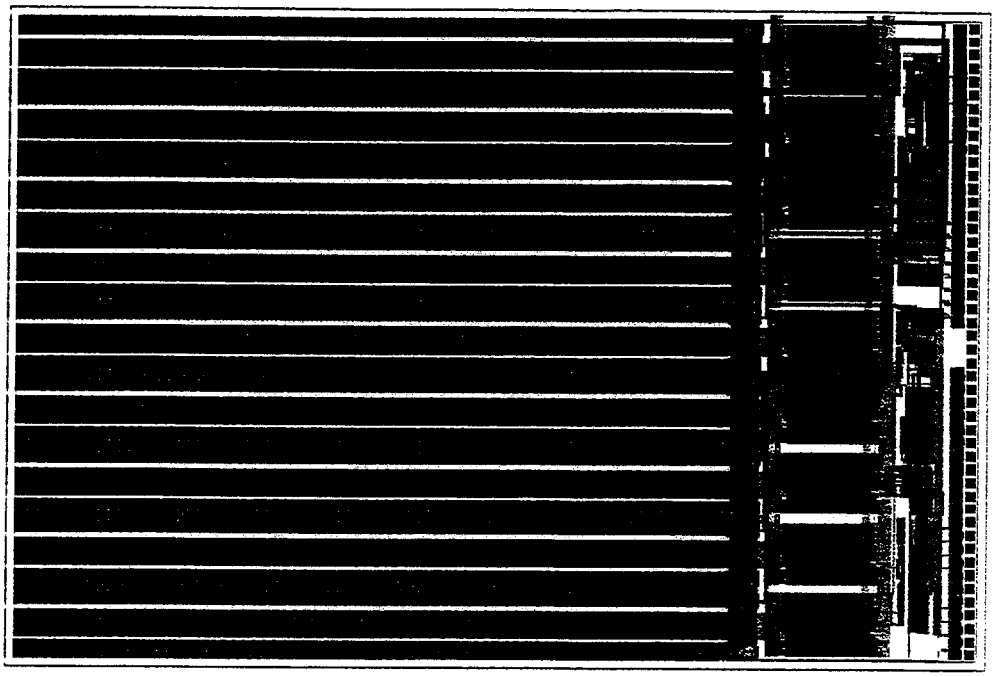
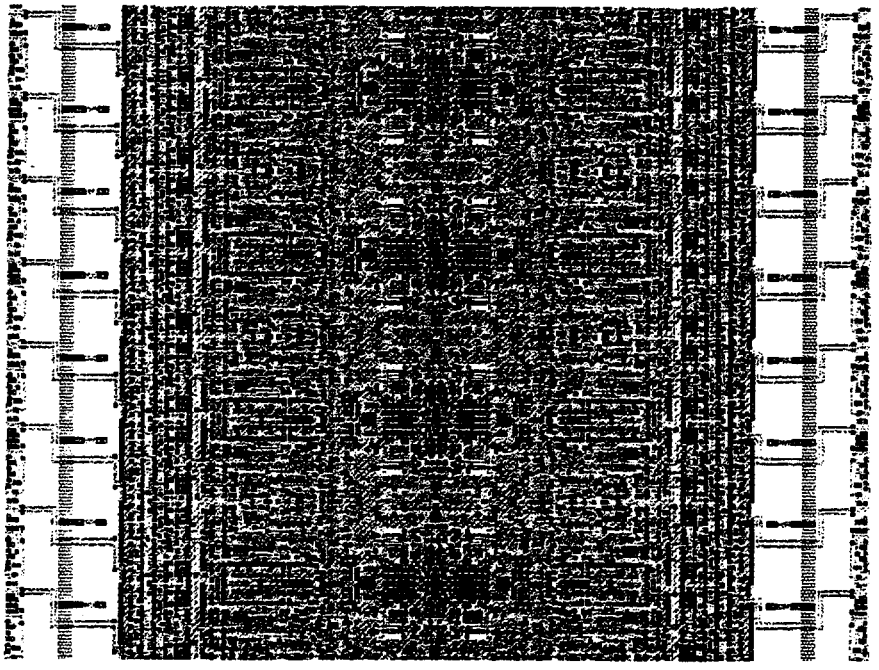
Complete Array

- Complete array includes roughly 837K transistors before merging:



Circuitry in Pixels:

- Analog front-ends, showing connection to digital back-end with empty zone between which contains substrate contact for digital logic:



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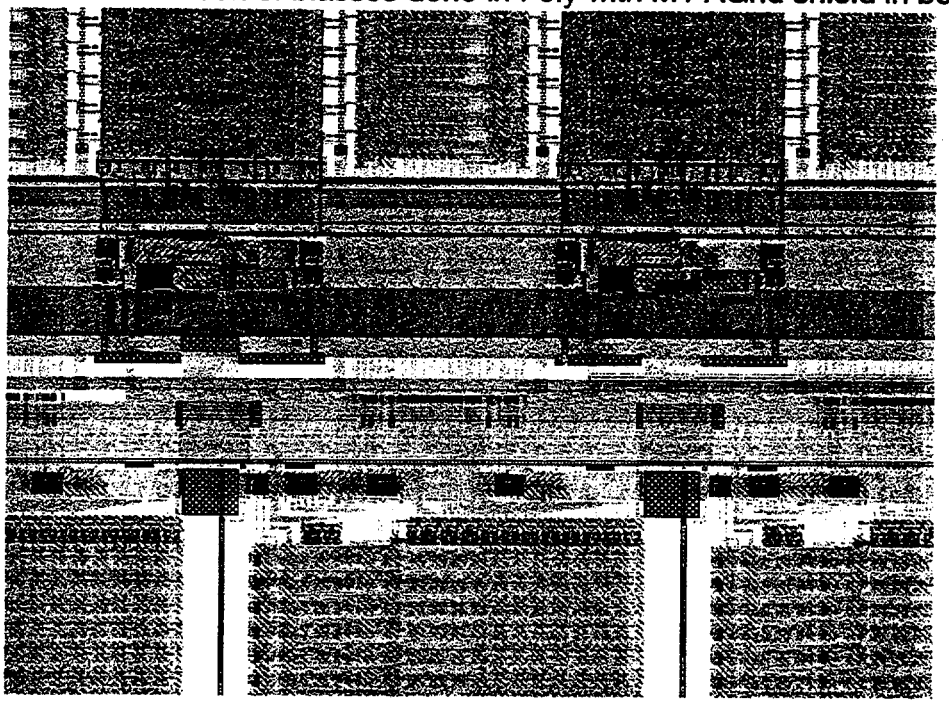
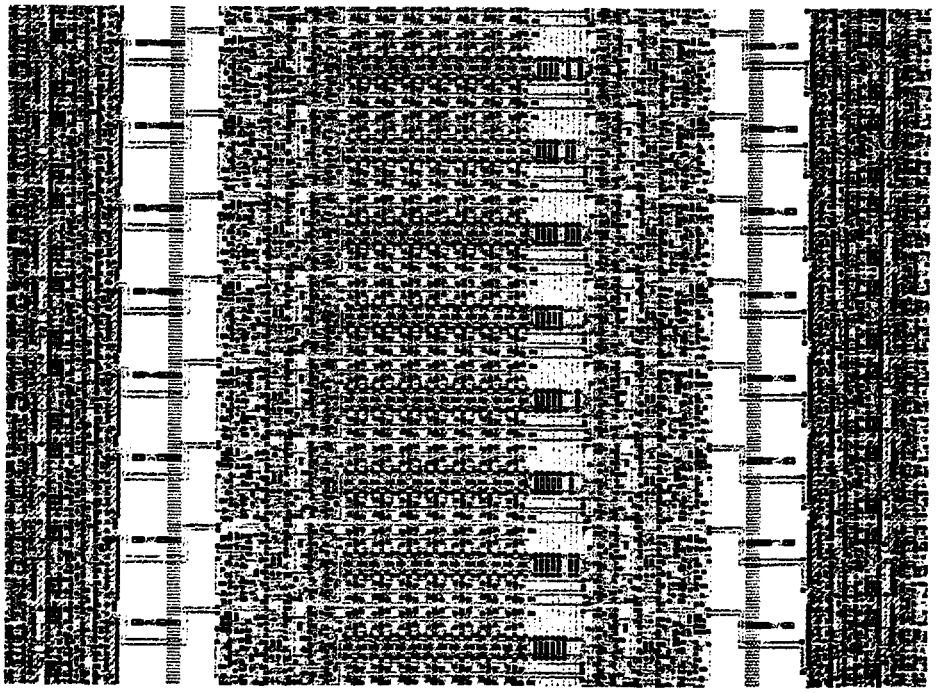
Bottom of Column Circuitry

- Contains active bias buffering and DAC circuitry (one DAC per column pair).
- Interleaving of circuitry: digital connections to pixel back-end are made in M2, horizontal distribution of biasses done in Poly with M1 AGnd shield in between:

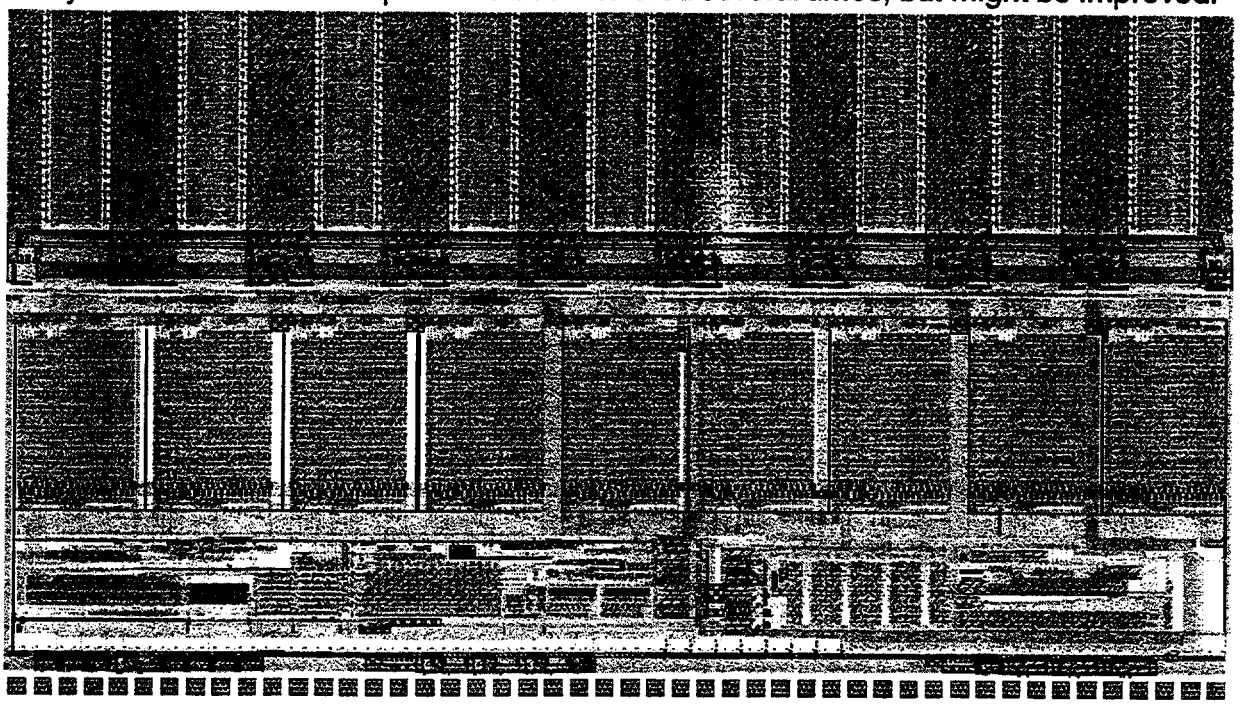


- Digital back-ends, showing extensive bussing to transfer data from pixels to EOC.
- This region is covered by an M3 shield which is brought out on Shield pin.



Bottom of Chip Circuitry

Bottom of the chip is quite full, with many routing details, making further compression very difficult. Present floorplan has been iterated several times, but might be improved:



VME-based Test System

High performance chips and modules need a high performance test system:

- Have developed a VME-based readout system, which supports one chip or module per VME card, and is hosted by a PC running LabWindows software.
- High performance "list processor" design, with an "instruction set" which supports basic operations in the system, e.g. FE-CONFIG, INT_DATA, EXT_DATA, etc. A simple linear "program" can be built using these atomic operations, and executed at high speed by an FPGA controller.
- I/O is through large parallel FIFOS, separate for command and data. A large local SRAM is provided to support "hardware histogramming" of the returning data, with one 256-bin histogram per pixel in a FE chip, with ID given by 13-bit Row/ Column. A detailed threshold scan can be performed in well under a minute.
- Provides a simple uniform interface for all control registers and operations in the system (local Control Card, MCC, and FE chips) which use different protocols and speeds.
- Does all parallel-serial conversions, word alignment, and simple data formatting at 40 MHz serial stream speed.
- Supports operation over 25m cable using PECL I/O and local connections using LVDS I/O for wafer probing, lab characterization, and testbeam readout.

Summary

Prototype pixel arrays have been operated at close to ATLAS requirements:

- Two parallel efforts have produced lots of measurements and new concepts, and demonstrated that LHC performance goals do seem achievable.

Realistic ATLAS prototypes are now being tested:

- We should have first operating modules (≈ 46K pixels each) by June 98.
- We expect to learn a great deal from these, particularly concerning the many system integration issues involved in module construction.

Next step is to submit "identical" chips to radhard foundries (both DMILL/TEMIC and Honeywell):

- This will give us experience with complete irradiated assemblies.

A final iteration (ATLAS2 chipset) will be developed before production begins:

- This gives us the opportunity to feed ATLAS1 radsoft and radhard experience into "pre-production" chips.

Real production should begin in 2000-2001...

The Module Controller Chip (MCC) of the ATLAS Pixel Detector

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Abstract

The ATLAS pixel detector is organized in 3 barrels and 5 forward and backward discs. The basic building block for each of those detector components is the detector module. There are a total of 2,228 modules, each one having 16 analog Front-End (FE) chips and a Module Controller Chip (MCC). Each module has 61,440 channels and must deal with a complex signal structure: 40 MHz event interaction rate, 75 kHz trigger rate and 2.5 μs trigger latency. The MCC has the main task to coordinate the 16 FE's: it does event building, handles errors and overflows and deals with trigger and synchronization signals. The ATLAS Pixel Collaboration is designing a radiation soft version of the detector module, as "demonstrator" of feasibility, before developing the final version.

This paper describes the MCC architecture and the prototype chip designed for the demostrator.

1. Introduction

The ATLAS pixel detector [2][3] is constituted of 3 barrel layers and of 5 forward and backward disks. Each barrel is organized into staves and each disk into sectors, both of which are in turn composed of modules. A total of 2,228 modules are used in the whole detector.

The read-out of the several thousand pixels hit amongst the $1.4 \cdot 10^8$ channels is a difficult problem.[4] To solve it, ATLAS has adopted a column-based read-out system because of its simplicity, and the high bandwidth operation provided by independent columns. High parallelism is maintained at each step of the read-out architecture together with apprpriate data compression. This is necessary to extract the extremely sparse information in the most efficient way. This read-out system is implemented using a tree-like structure with distributed intelligence at each node.[5]

2. Module

A perspective view and a simplified block diagram of the module are shown in Figure 1 and Figure 2. The two different blocks in Figure 2 are the *Front-End* (FE) chip, which is replicated 16 times, and the *Module Controller Chip* (MCC). The interconnections have been kept very simple, and all connections which are active during data-taking use low-voltage differential signalling (LVDS) standards to reduce EMI and balance current flows. Other signals use full-swing single-ended CMOS to reduce the pin count.

The interconnect topology between the MCC and the 16 FE chips in a module is a star topology using unidirectional serial links. This topology has been chosen to improve the tolerance of the system to individual component failure, as well as to improve the bandwidth by operating the serial links in parallel.

The ATLAS Pixel Collaboration is currently designing a "detector module demonstrator" which implements the final functionality required for the experiment, but with two main exceptions: it has slightly larger pixel cells (400 x 50 μm^2 instead of 300 x 50 μm^2), to leave adequate room for diagnostic and control logics, and it has electrical instead of optical inputs and outputs. In addition, the chips on the current built module are designed in radiation-soft technology.

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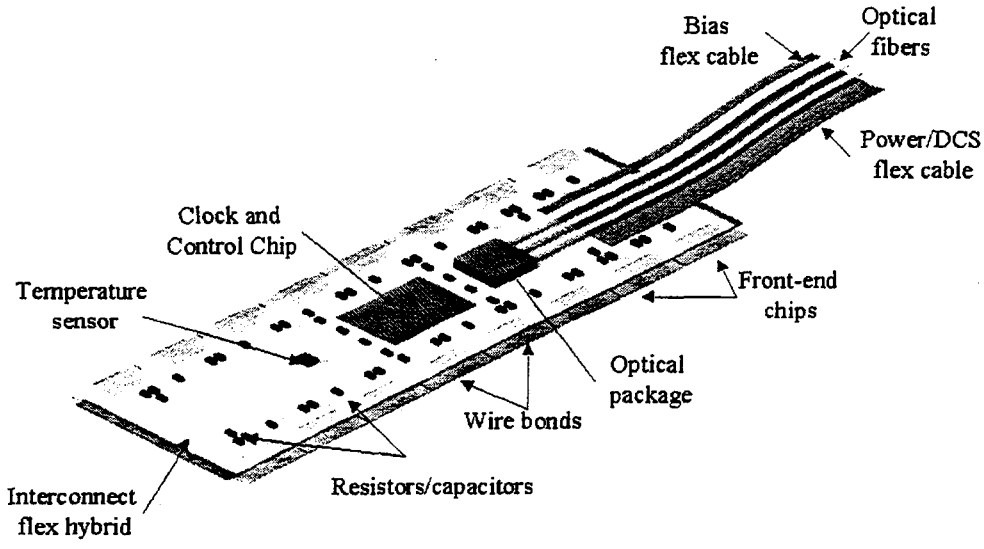


Figure 1: Perspective view of a detector module.

The prototyping effort for the demonstrator is being pursued with the aim of providing two front-end chip designs in rad-hard technologies using two different vendors, according to the official ATLAS policy for rad-hard electronics development. The two front-end designs (FE-A and FE-B) differ in many internal details, but are intended to be "functionally pin-to-pin compatible", so that modules can easily be built with either front-end chip and comparatively tested.

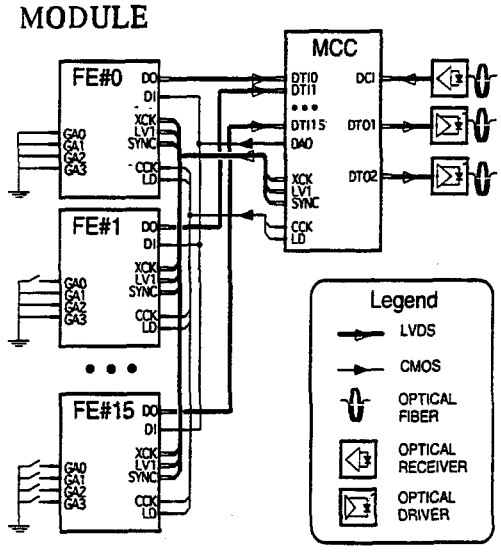


Figure 2: Module block diagram

Both FE chips have 18 columns (will be 24 with the pixels shrinking to 300 μm) and 160 rows of pixel cells. Every second column is mirrored and the architecture for the *End-of-Column* (EoC) logic is organized for a column pair. Both pixel front-ends will provide modest digital information using a time-over-threshold (TOT) front-end design, and digitizing the charge information in units of the 40 MHz beam crossing rate.

3. MCC System Architecture

The MCC has 3 main functions: event readout and building, FE chip configuration and trigger and timing distribution to the FE chips.

3.1. Event Readout and Event Building

The first significant event building occurs in the End-of-Column (EoC) logic on the Front End chip, where data are organized into events labelled by 4-bit trigger numbers. These events are then pushed from the FE chips to the MCC as soon as each FE chip has a complete event. The MCC collects the parallel data

streams from all of the FE chips and performs real event building. It then transmits these events to the ROD (Read Out Driver). The final event building tasks is left to the ROD's, where power and space are not as constrained as they are on the detector.

The End-of-Column logic receives input from a pair of pixel columns. All pixel hits are stored in the EoC buffers until a level one trigger (LV1) coincidence is performed. After that, only hits associated with a triggered beam crossing are kept and are transferred off the FE chip into the MCC. These basic operations, namely hit storage, LV1 trigger coincidence, and event readout, must be simultaneously performed by the EoC logic in order to prevent generating significant inefficiencies. Each FE chip uses a 4-bit trigger number to uniquely label events which are awaiting readout into the MCC. The MCC has the ability to suppress additional LV1 trigger signals if the number of LV1 triggers sent to the FE chips exceeds *n* (where *n* can be programmed from 1 to 15). This number represents the maximum number of events that a single FE chip can store.

The high luminosity of LHC forces an "*as-quickly-as-possible*" approach in getting data transferred from hit pixels to the End-of-Column buffers. This process causes data entering the EoC buffers to become somewhat scrambled, and will therefore no longer be organized sequentially into events. Hence this buffer will not behave as a FIFO, and data from a given event will not be stored contiguously. It becomes therefore necessary to scan the EoC buffer pool in order to find the next free location prior to writing new data. The buffer pool has also to be scanned a second time to find all the hits corresponding to a given event in order to provide the MCC with data ordered by event.

Event building is performed by two concurrent processes running in the MCC. The first (*Receiver*) deals with the filling of the 16 input FIFO's with data received from the corresponding FE chips, while the second one (*Event Builder*) extracts data from the FIFO's and builds up the events. Each FE chip sends data as soon as they are available with two constraints: event hits must be ordered by event number and for each event an `End-of-Event` (*EoE*) word is always generated. *EoE* is also sent for the case of an empty event to keep event synchronization.

Each time an *EoE* is received by a *Receiver* in the MCC this information is stored in a "score board". Therefore the *Event Builder* knows exactly when to start the event building by checking the "score board" which keeps track of which events are completely

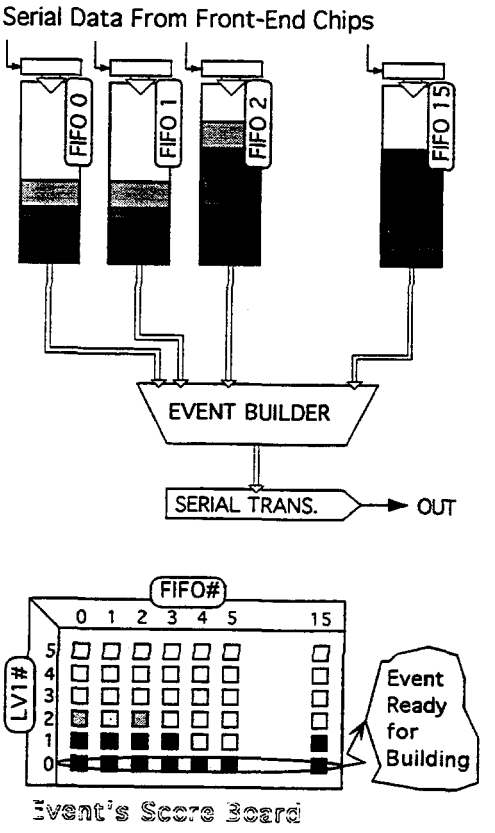


Figure 3: Event "Score Board" used in the MCC for event building.

stored in each of the 16 input FIFO's. When an event flagged with LV1 number *n* is ready in all the FIFO's the *Event Builder* process takes all the hits from FIFO#0, appends them to that of FIFO#1, and so on up to the last FIFO#15. At the end of this process the corresponding "score board" entry is erased. While the *Event Builder* fetches the hits out of the FIFO's, the MCC transmits them upstream to the *optical encoder*. The event number is removed from each hit and sent only once, together with the FE chip addresses, to the ROD. The event building score board is sketched in Figure 3.

The block diagram of Figure 4 is an expanded view of one of the sixteen FIFO's of Figure 3. During normal conditions, the RECEIVER fills data into the FIFO. When an *EoE* word arrives, CTRL copies the contents of W.PTR (Write Pointer) into L.PTR (Last Pointer). When the Event Builder finds that an event is completely received from all of the 16 FE chips

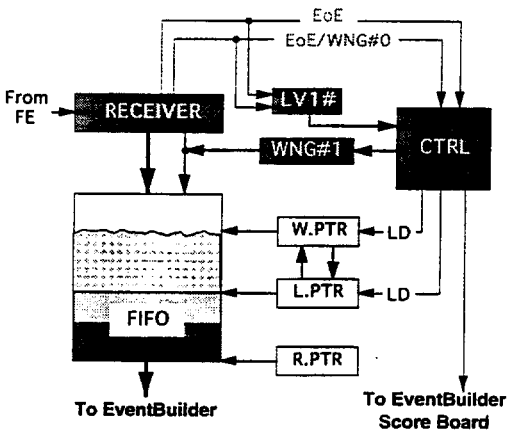


Figure 4: Event readout: Front End RECEIVER and input FIFO.

(*Event Builder* knows from the scoreboard about the existence of complete events) it starts fetching data. After every FIFO read operation its R.PTR is incremented. R.PTR will never overtake L.PTR and the *Event Builder* can start processing the next FIFO once it finds an *EoE* in the data.

The MCC is able to handle both warning and error conditions during event building. A `warning` occurs when there is a condition which causes a partial event loss. An `error` is a destructive condition that cause the loss of one or more events until the MCC recovers. Both `warning` and `error` conditions are flagged in the output data stream. Due to the data push architecture, the overflow of an input FIFO could always occur: the mechanism the MCC uses to resolve such a condition is to issue a `warning` or an `error` condition.

3.2. System Initialization and Configuration

Front end chips and MCCs must be configured after power up or before starting a data taking run. This is done by a system initialization procedure. To write or read configuration data to/from the FE chips, two levels of addressing are necessary:

1. The data path to the given module must be selected.This is done by selecting the I/O port on the ROD corresponding to the module on which the target FE chip resides. The ROD uses point-to-point links to the MCC's for both input and output connections.
2. The FE chip must be addressed. This is done by the FE chip itself, which recognizes its geographical address in the Command plus Address field of the message. Once the address is recognized, the remaining data stream will be used by the FE chip either to execute the command or to upload/download internal registers. Since all of the information going to the FE chips must pass through a MCC chip, the MCC must recognize whether the data is for its own use or must be transferred to the *MCC-DAO* (Data Address Out) pin of the FE port, which is connected to the FE chip inputs (see Figure 2). This is done by looking at the secondary address field present in the header field of the message.

Data streams sent to (or returned from) the FE chips have variable length. When writing, this length must fit the size of the relevant internal FE registers. To ease the FE chip design for the demonstrator chips, configuration data are transmitted at a reduced 5 MHz bit rate, using the *MCC-CCK* clock, instead of the 40 MHz used for event readout. Experience will tell us whether this can be eliminated in the next generation of chips.

To simplify the control decoder the *MCC-LD* signal is used to distinguish, in the bit stream from the *MCC-DAO* pin, the address plus control words from the subsequent data words.

The MCC architecture foresees up to 16 general registers which can be written and read back during system configuration. Two of them are used to define the length, respectively of the `data` and of the `control` part, in the bit stream which will be sent to the FE chip. The MCC registers support both system control functions and access status information that is particularly useful at debugging time.

3.3. Trigger, Timing and Control

During normal operation, the on-detector electronics of the pixel system needs a precise timing signal (XCK - Bunch Crossing Clock) and a trigger signal (LV1 - Level 1 Trigger). In addition to those two signals several control commands are understood by the system. The main signals are:

- XCK (Bunch crossing clock)

  This is the clock seen by the FE chip on its *FE-XCK* input line. XCK is generated from the 40 MHz clock signal received by the MCC through the *DCCI* input pin. The 40 MHz clock signal and *FE-XCK* both have the same frequency as the LHC machine clock. Each detector module uses the same 40 MHz clock, but a small phase

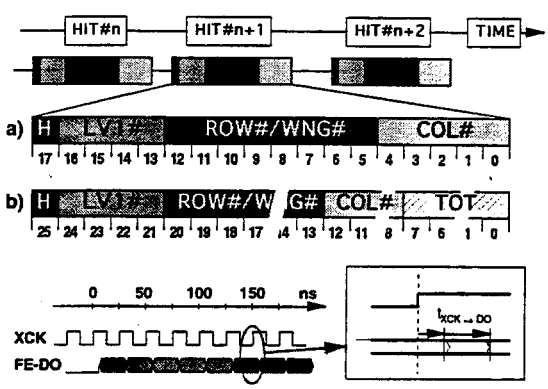


Figure 5: Hit Data format at the input of the MCC. Case b) illustrates the Time over Threshold encoding.

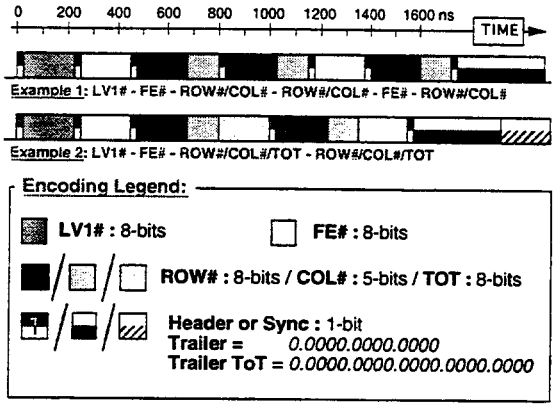


Figure 6: Event Data format at the MCC output. Example 2 illustrates the case of Time over Threshold encoding.

difference can be programmed in the ROD to take into account timing differences. The XCK signal is used by pixel Front End to latch and associate track hits to a particular bunch crossing number.

- LV1 (Level 1 Trigger)

  This signal validates the rising clock edge of the bunch crossing clock (*FE-XCK*) for those crossings that have been accepted by the level 1 trigger system. The serial control protocol is used to transmit the LV1 command from the counting room down to the MCC, where it is received serially encoded on the *MCC-DCCI* pin. Once received by the MCC this signal is decoded by the *Command Decoder* inside the MCC and distributed to all the FE chips. One of the features of the MCC is the ability to generate a pattern of contiguous LV1 Accept signals to allow possible multi-crossing read-out, both for diagnostic and timing initialization, and to allow for the possibility that all of the interesting hits may not be available in a single beam crossing. Hits belonging to triggered bunch crossings cause data to be stored by the End-of-Column logic in the FE chips and subsequently pushed to the MCC. The MCC puts together hits from the same event and pushes them to the ROD's.

- SYNC (Event Synchronization)

  This signal is used to automatically re-synchronize all FE chips in a module in case of error conditions. The MCC can generate this signal autonomously whenever the particular module is empty, or when it detects an error condition. It can also receive a SYNC command from the ROD. In the first case all the FE chips on the module controlled by the MCC which issued the SYNC reset their internal LV1 counter and delete any pending triggered event. The FE chips will then resume data taking and pushing as soon as they see the next LV1 signal. In a similar way, all MCC's respond to a SYNC sent by the ROD by resetting all FE chips connected to them and resetting the LV1 counter and data inside the FIFO's once as many pending events as possible have been reconstructed. The MCC then sets a warning condition in this events data streams.

- Slow Commands

  These commands are used to program the MCC or the FE chips in a particular module. When one of these commands is issued, the pixel system is taken out of data acquisition mode, and command operations like system configuration or read/write operations can be executed at any level of the hierarchy. There is a Data-Take command in order to resume data taking.

4. Data Formats

Data will be transmitted from the FE chip to the MCC using a simple protocol in which each hit is transmitted in a stream of 18 bits (26 if the optional Time-over-Threshold (ToT) information is produced): 1 header bit, 4 LV1 bits, 8 row number or end-of-event/warning bits, 5 column number bits and 8 optional ToT bits. Individual hits can be separated by any number of zeroes in the data stream. The average occupancy of the link is expected to be fairly low. This, together with the encoding scheme

described here, permits automatic recovery after data transmission errors, so long as a gap longer than 18 (or 26 in case the ToT option is selected) bits appears in the data stream. The data encoding and transmission is represented in Figure 5.

The format of the event generated by the MCC is made of ordered fields separated by synchronization bits ("1"), starting with a header ("1") and ending with a trailer ("100 0000 0000 0000"). The header is to "wake up" the receiver from the idle condition when no data are transmitted, while the synchronization bits together with the trailer are used to define the end of event. The trailer has been chosen to be a pattern that can never occur in the data stream, due to the insertion of synchronization bits. The format always requires a LV1 number at the beginning followed by a sequence of FE chip numbers, followed by any number of hits (row plus column or row plus column plus ToT when this option is selected) interrupted by a new FE chip number plus the sequence of hits. Warning and error flags can be introduced in the event format. An example of such a format is given in Figure 6.

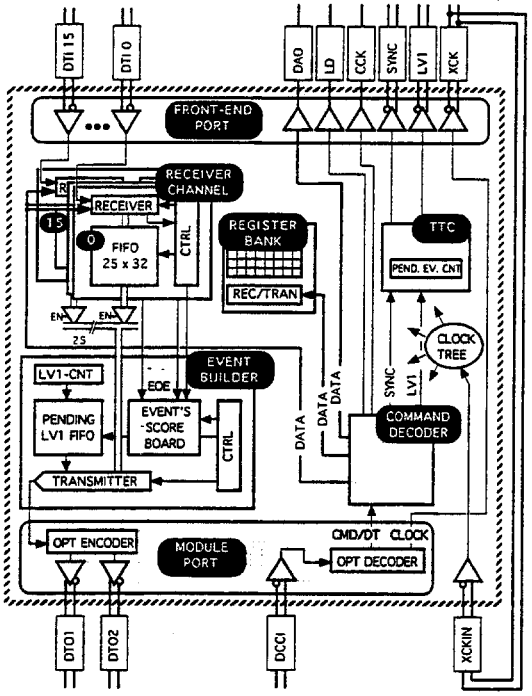


Figure 7: MCC Block Diagram.

5. MCC Architecture Implementation

The MCC architecture is shown in the block diagram of Figure 7. The blocks represented are:

FRONT END PORT: (I/O to the FE chips)
This module performs all of the interface functions between the FE chips and the MCC.

RECEIVER CHANNEL: (Front End receiver)
This block includes the 16 derandomizing FIFO's (one for each FE chip output), made with a full custom memory of 32 25-bit long words with arbitration logic and read/write pointers, and the FE receivers and the state machine running the interface to the FE link. FIFO overflows are handled by this block.

EVENT BUILDER:
A scoreboard keeps track of complete events read by each FE chip. Once all 16 FE chips have sent a complete (even empty) event, the *Event Builder* sorts, formats and prepares the event stream to be transmitted to the RODs once encoded by the *Module Port*. Errors at the level of event building are dealt with by this block. Both `error` and `warning` conditions are added in the output data stream if necessary.

REGISTER BANK:
The MCC architecture provides up to 16 general purpose registers, only 11 of which have been implemented in the demonstrator MCC. As an example, a register is used to mask one or more input lines coming from FE chips in case of failure. Two special registers contain the bit length of commands and data to be written to the Front End chips as these quantities may vary each time a FE chip is accessed.

COMMAND DECODER:
This block decodes all commands sent to the MCC. The LV1 trigger command (fast command), as well as read/write operations to internal MCC registers or to FE chips (slow commands) are amongst the commands interpreted by this block.

TTC: (Trigger, Timing and Control)
This block generates the LV1 trigger to the FE chips. It has the ability to block LV1 accepts to all of the FE chips on a module if there are too many LV1 events still to be transmitted to the MCC. This block therefore keeps track of all LV1 signals sent to the FE chips and all the Event-Done signals received by the Event Builder. One of the functions of this block is to deal with the automatic Sync signal programmable into the MCC or received by the RODs via a dedicated command.

MODULE PORT: (Interface to the ROD's)
This module performs all of the interface functions between the MCC and the RODs. Clock and serial commands are decoded and sent respectively to the *Clock Tree* and the *Command Decoder* block. Outgoing signals are encoded with the clock and are sent out on *MCC-DTO1* and *MCC-DTO2* pins according to bandwidth requirements. Bandwidth requirements predicate the use of three optical fibres.

CLOCK TREE:
Once the clock has been decoded by the *Module Port*, it must be distributed to the whole module. In order to minimize clock skew between the MCC and the FE chips, the MCC generates the clock and latches all input/output data with this clock signal. This signal is then sent to all the components of the module via the *MCC-XCK* output pin. The MCC itself will use this distributed clock for all its internal operations.

The MCC chip will be fabricated in rad-hard technology using the DMILL 0.8 µm double metal CMOS process. To minimize the risk of errors in the rather complex MCC design, a top-down design methodology has been used, using standard cells with logic synthesis from a high level Verilog description. The only full custom parts of the design will be the 16 FIFO's, the LVDS I/O drivers/receivers and the Bi-phase Mark Encoding and Decoding blocks, which do not exist in the DMILL standard cell library.

6. MCC for the ATLAS "Demonstrator"

Since the demonstrator module does not have optical links, the main differences between it and the final version are the absence of the Bi-phase Mark Encoding and Decoding blocks which will be added to the Module Port (see Figure 8). Another difference is that this version of the chip has been produced in rad-soft technology using the AMS 0.8 µm double metal CMOS process.

Due to the complexity of the circuit a top-down design methodology has been chosen. The whole design was first coded in Verilog at a behavioural level, and then mapped to the 3.3 V, 0.8 µm CMOS AMS standard cell library using a logic synthesis tool (Synergy), with the exception of the full-custom blocks. After hand-positioning the custom blocks, the layout was made with an automated place and route tool. The final steps of this process were the layout versus schematic comparison and the design rule check. The whole design was made using the Cadence Design Framework. Figure 11 presents the final

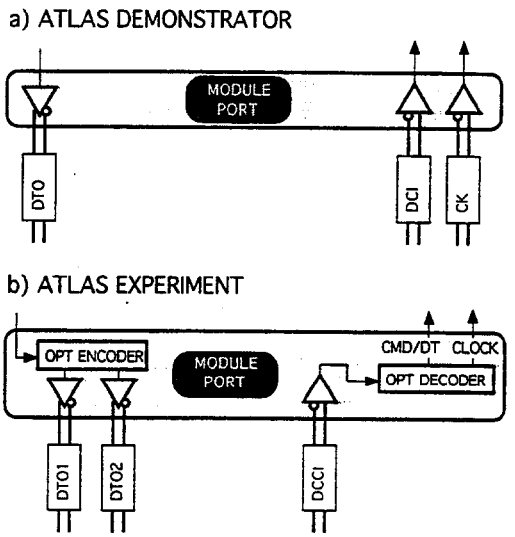


Figure 8: Difference between the "Demonstrator" MCC (a) and the MCC which will be designed for the experiment (b), The final chip will receive clock and data encoded on a single fiber (DCCI), while two output fibers will be used to increase the bandwidth (DTO1 & DTO2).

layout with the main building blocks highlighted. Approximately half of each receiver channel foot print is occupied by a FIFO.

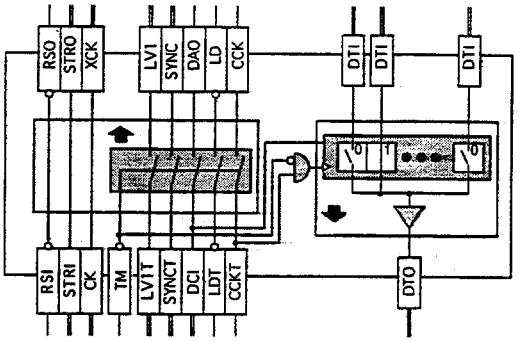


Figure 9: Block diagram to illustrate the "Transparent Mode" operation of the MCC.

Since the 16 FE chips in a module will be accessed through the MCC by a rather complex protocol, we have added a "Transparent Mode" of operation to the MCC. This mode requires the addition of several pins and a small amount of logic, but allows transparent access to all input and output pins of the 16 FE chips. This operational mode bypasses all of the MCC

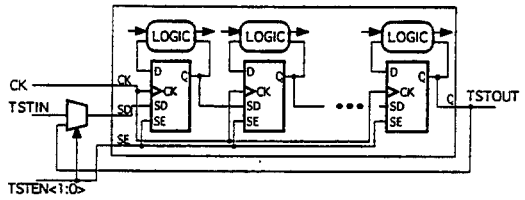


Figure 10: Scan chain to access in read and write mode MCC internal flip-flops.

functionality and directly connects all data, control and timing signals going to (or returning from) the FE chips with corresponding externally accessible pins on the MCC.The Figure 9 shows the implementation of the "transparent Mode" in the MCC.

The MCC has additional pins which can be used to put the circuit into test mode and increase the accessibility and observablity of internal nodes. In this test mode all the internal flip-flops are configured as a shift register, see Figure 10, which allows both reading and writing the MCC internal state. This mode will be used to test the chip on a probe station before mounting it in the system.

The MCC has 60 signal pins, and with the inclusion of power and test signals, there will be a total of 81 pins on the chip die. The chip area is 67 mm^2 and has approximately 430,000 transistors. The design will not be optimal in its area and power consumption, but this approach provides the safest route to produce the MCC prototype on this short time scale.

The MCC is in fabrication in an engineering run, and we will receive functionally-tested chips, in order to facilitate the assembly steps of the whole module. A first test of the whole module should take place in August 1998 in the CERN H8 test beam.

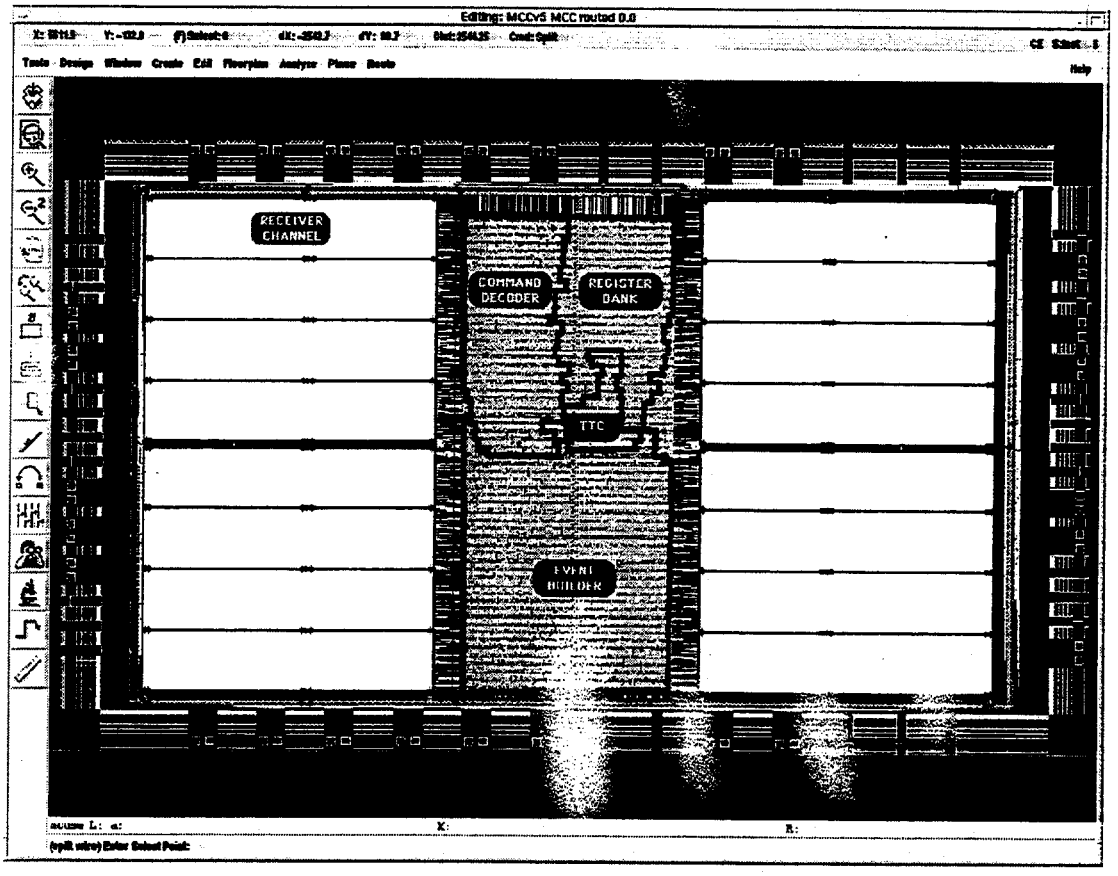


Figure 11: MCC layout. The different functional blocks have been highlighted.

Aknowledgments

I wish to thank the co-authors of the MCC demonstrator chip design: R. Beccherle, G. Comes, G.Gagliardi, G. Meddeler and P. Musico.

References

[1] ATLAS Pixel Collaboration: M. Ackers, M. S. Alam, M. Aleppo, E. Anderssen, A. Andreazza, B. Athar, D. Barberis, R. Beccherle, C. Becker, K.-H. Becks, D. Bintinger, L. Blanquart, W. Boyd, A. Brandl, G. Cabras, M. Caccia, D. Calvet, C. Caso, D. Cauz, E. Charles, S. Ciocio, J-C. Clemens, D. Cobai, G. Comes, M. Dameri, J. Dailing, G. Darbo, S. D'Auria, A. De Angelis, B. De Lotto, C. del Papa, P. Delpierre, D. Dorfan, J. Drees, T. Dubbs, K. Einsweiler, J. Emes, T. Fahland, D. Fasching, P. Fischer, G. Gagliardi, Y. Gally, C. Geich-Gimbel, C. Gemme, P. Gerlach, M. Gilchriese, K.W. Glitza, M.S. Gold, S. Gonzalez, G. Gorfine, C. Gößling, I. Gregor, A. Grillo, P.Gutierrez, O. Hayes, G. Hallewell, M. Hoeferkamp, M. Holder, F. Hügging, R. Jared, A. Joshi, M.Keil, S. Kersten, S. Kleinfelder, R. Kluit, M. Kobel, Z. Kohout, T. Kuhl, A.J. Lankford, R. Leitner, G. Lenzen, C. Linder, Z. Ling, A.K. Mahmood, R. Marchesini, J.A.J. Matthews, F. McCormack, T. McMahon, G. Meddeler, C. Meroni, S. Meuser, O. Milgrome, P. Morettini, T. Mouthuy, P. Musico, J. Nachtman, K. Neiyanuri, W. Ockenfels, M. Olcese, B. Osculati, N. Palaio, Y. Pan, F. Parodi, F. Pengg, S. Pier, E. Piotto, P. Polevin, R. Potheau, A. Pozzo, F. Ragusa, J. Richardson, G. Ridolfi, T. Rohe, L. Rossi, A. Rozanov, H.F.W. Sadrozinski, L. Santi, R. Schoefer, I. Scott, F. Scuri, S.C. Seidel, A. Seiden, G. Sette, H.S. Severini, P. Skubic, P. Sicho, P.K. Sinervo, J. Snow, B. Sopko, E. Spencer, D. Stoker, M. Strauss, L. Stupka, J. Thadome, S.C. Timm, L. Tomasek, J. Treis, W. Trischuk, C. Troncon, V. Vacek, I. Valin, B. van Eijk, G. Vegni, E. Vigeolas, V. Vrba, F. Waldner, F.R. Wappler, N. Wermes, S.L. Wu, R. Wunstorf, J. Wüstenfeld, M. Ziolkowski, G. Zizka, H. Zobernig.

[2] ATLAS Pixel Detector Technical Design Report, CERN/LHCC/98-13.

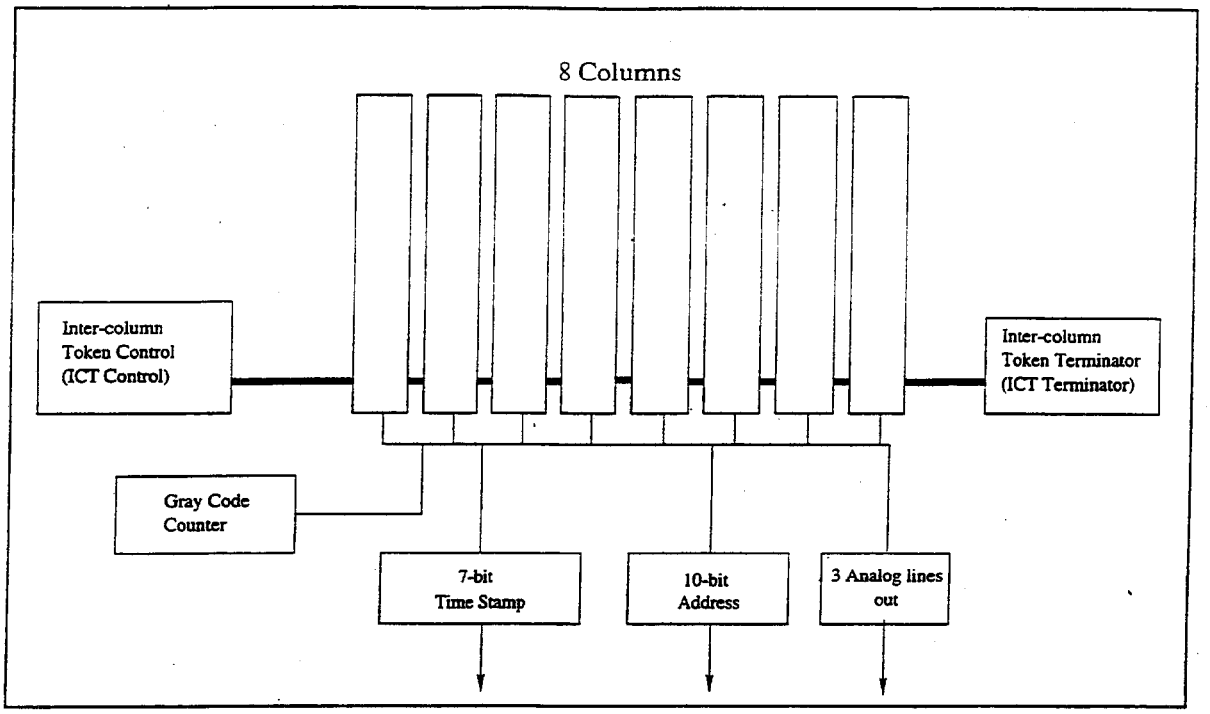
[3] G. Gagliardi, The ATLAS Pixel Detector, these proceedings.

[4] G. Darbo, The ATLAS Pixel Detector System Architecture, Proceedings of the "Third Workshop on Electronics for LHC Experiments", CERN/LHCC/97-60.

[5] G. Darbo et al., "ATLAS Pixel Demonstrator: Pixel Electronics Specification", ATLAS INDET Note in preparation, http://www.ge.infn.it/ATLAS/Electronics/home.html.

BFE 168

Chip Level Diagram

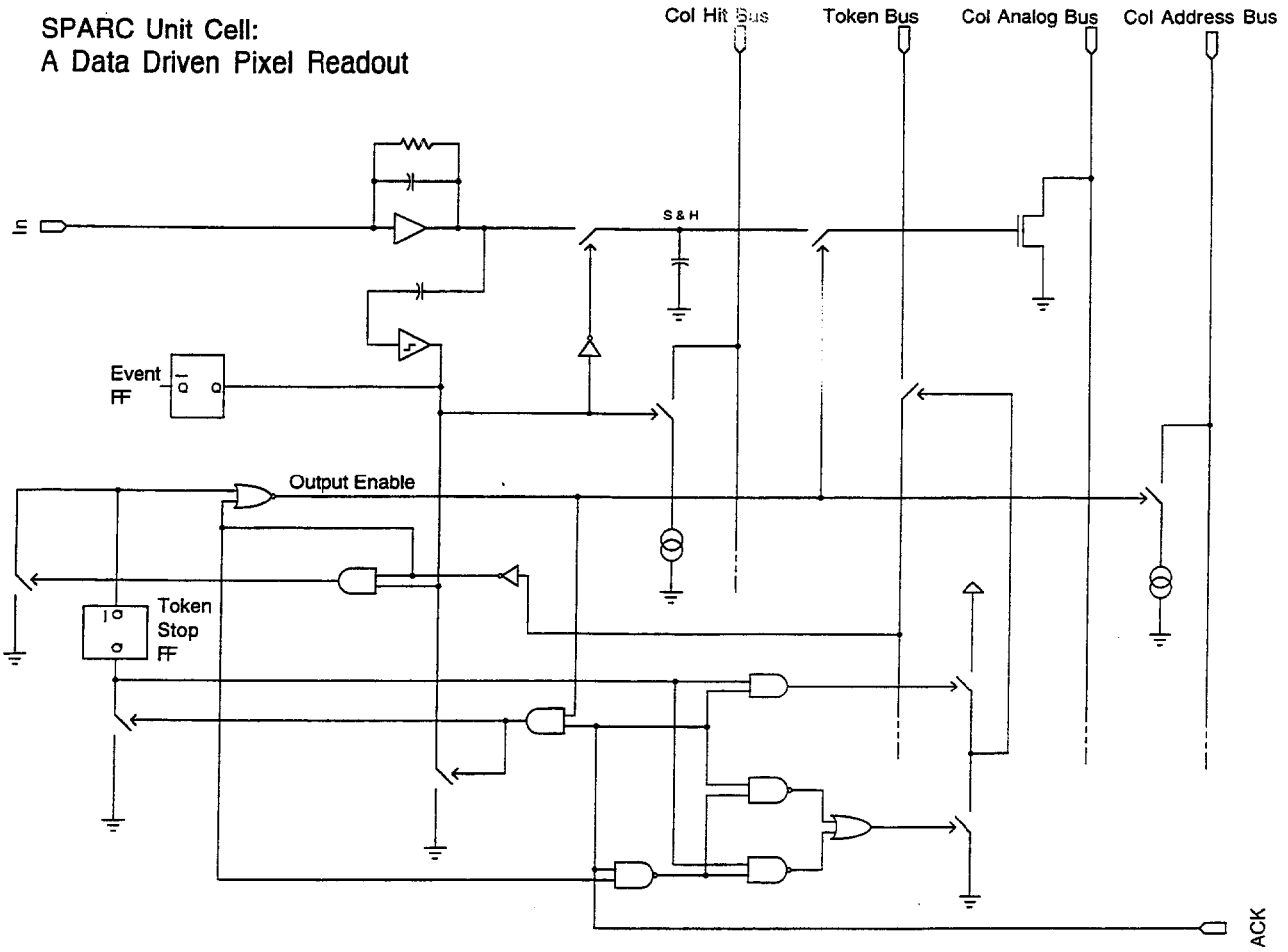


Results from a Pixel Readout Chip for CMS

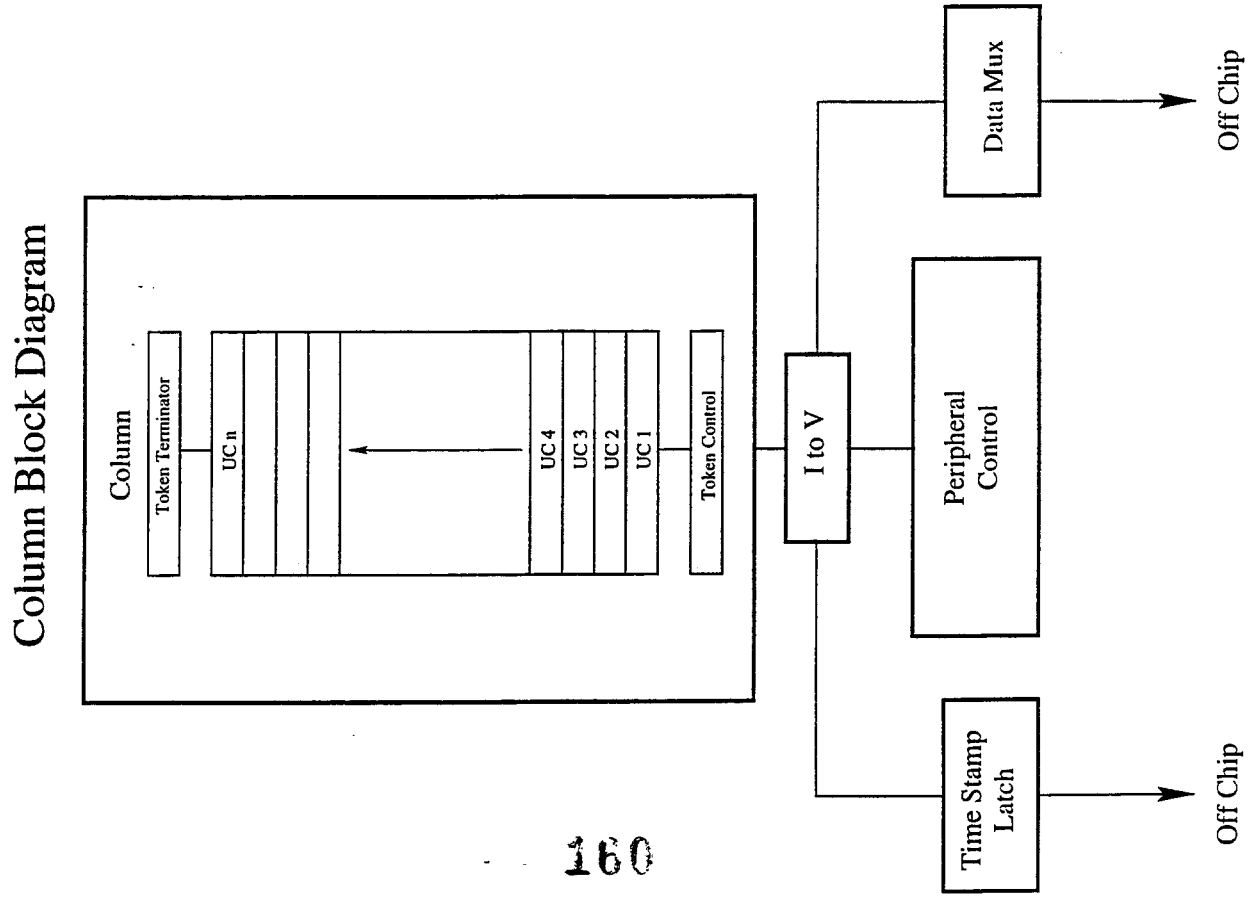
Gary Grim

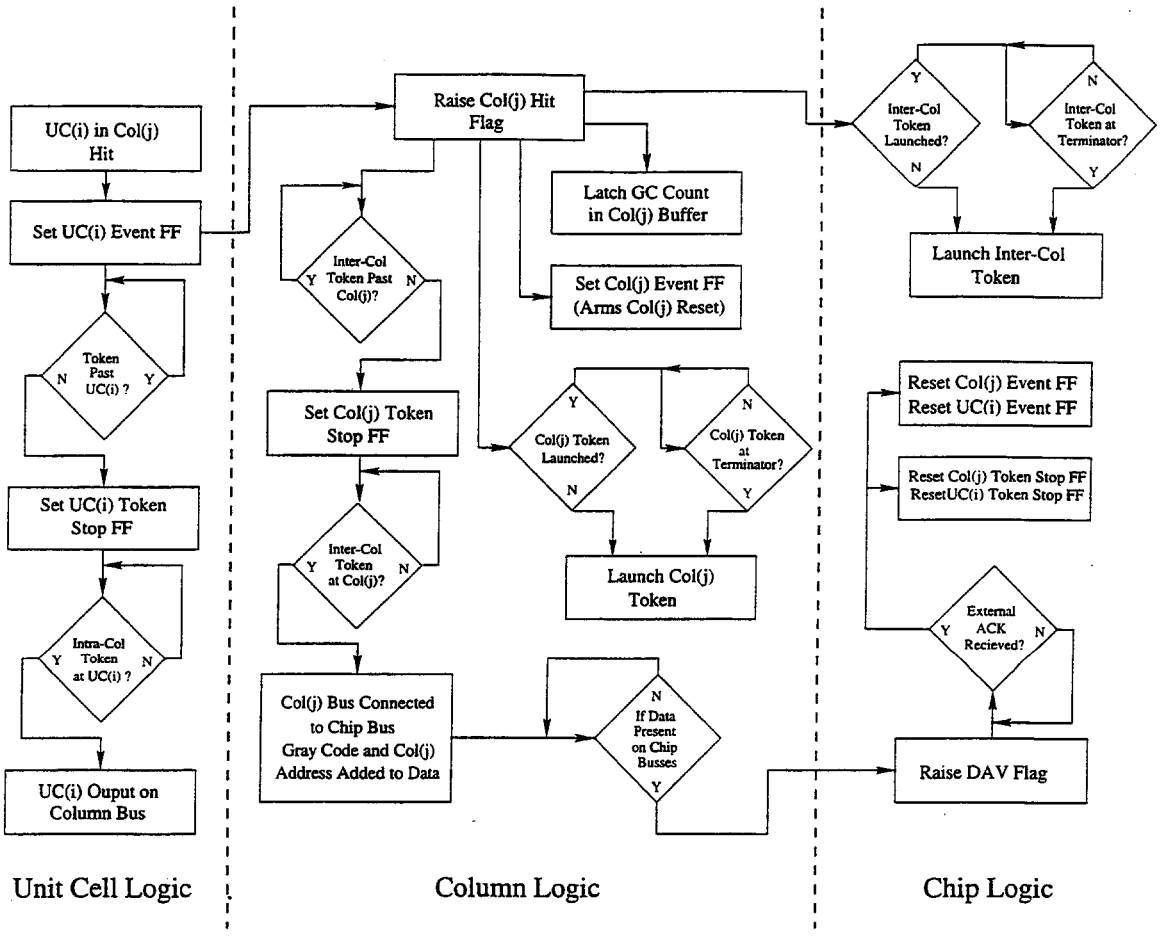
UC Davis

SPARC Unit Cell:
A Data Driven Pixel Readout

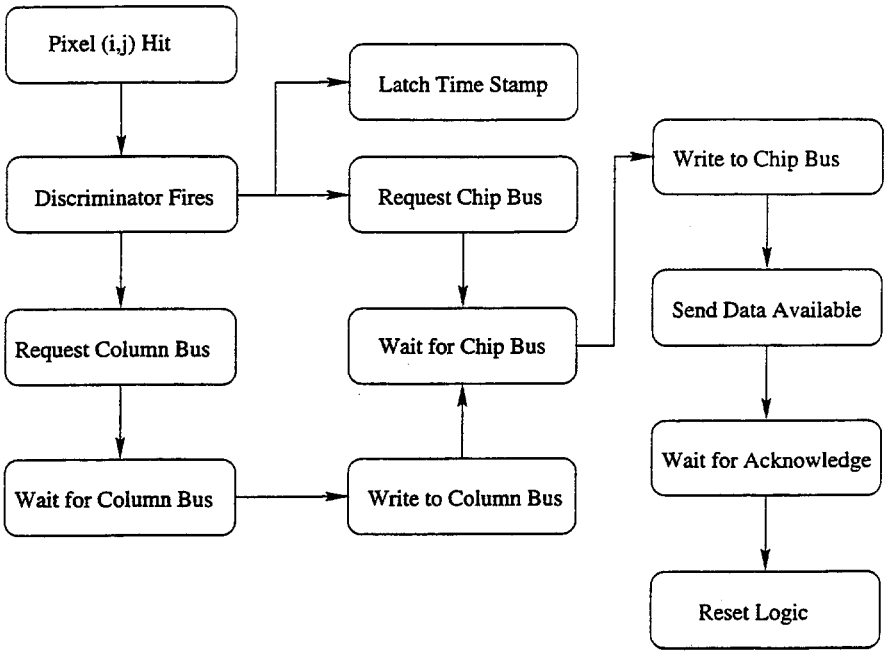


Column Block Diagram

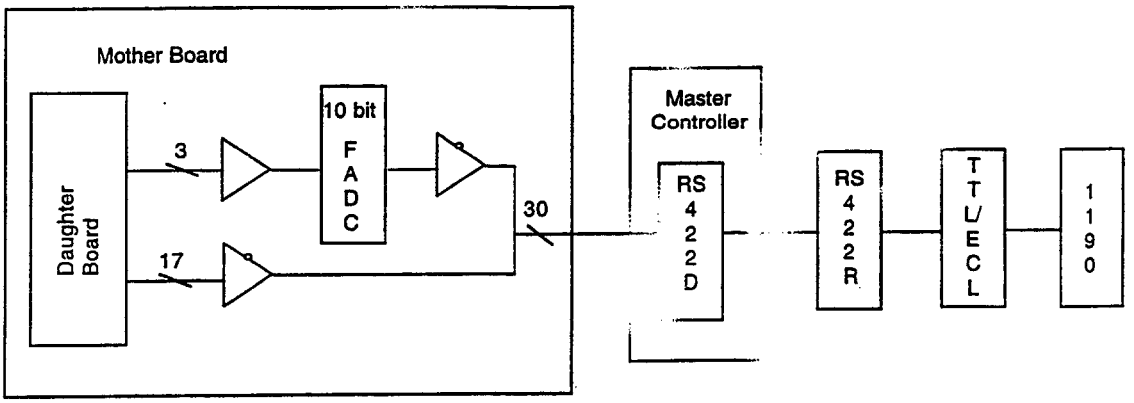


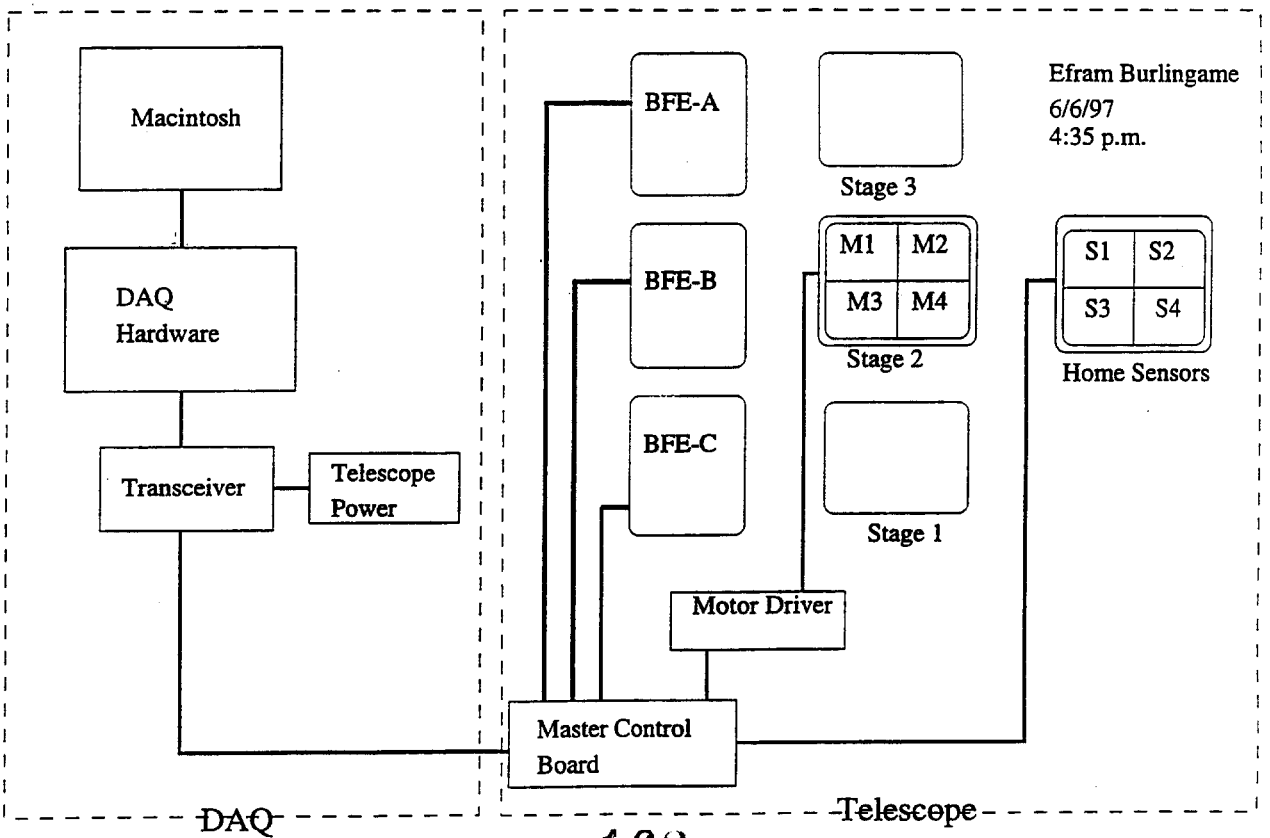


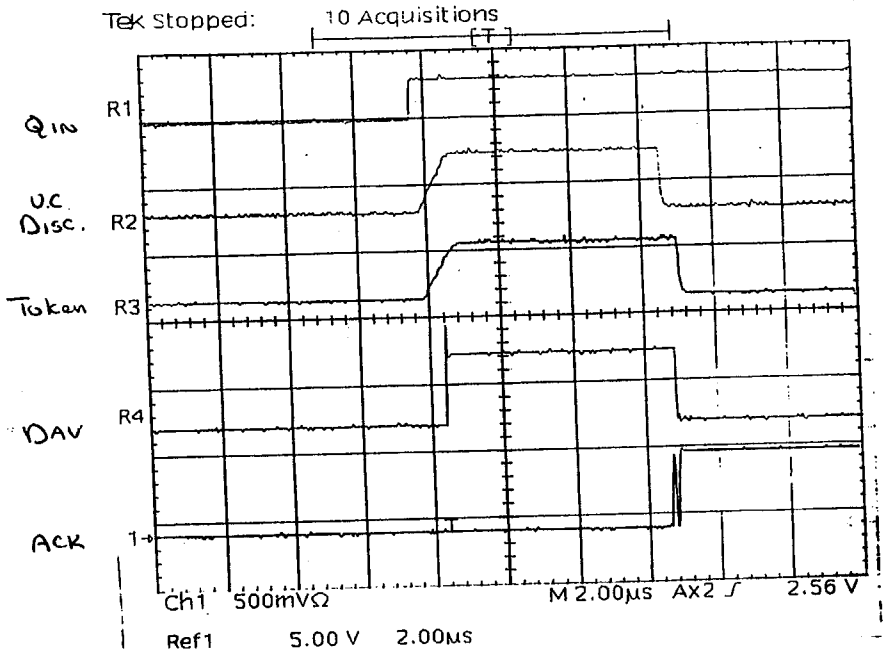
BFE-168 Data Flow



Data Path


Mother Board
Daughter Board
3
17
10 bit
F
A
D
C
30
Master Controller
RS 422D
RS 422R
TTL/ECL
1190

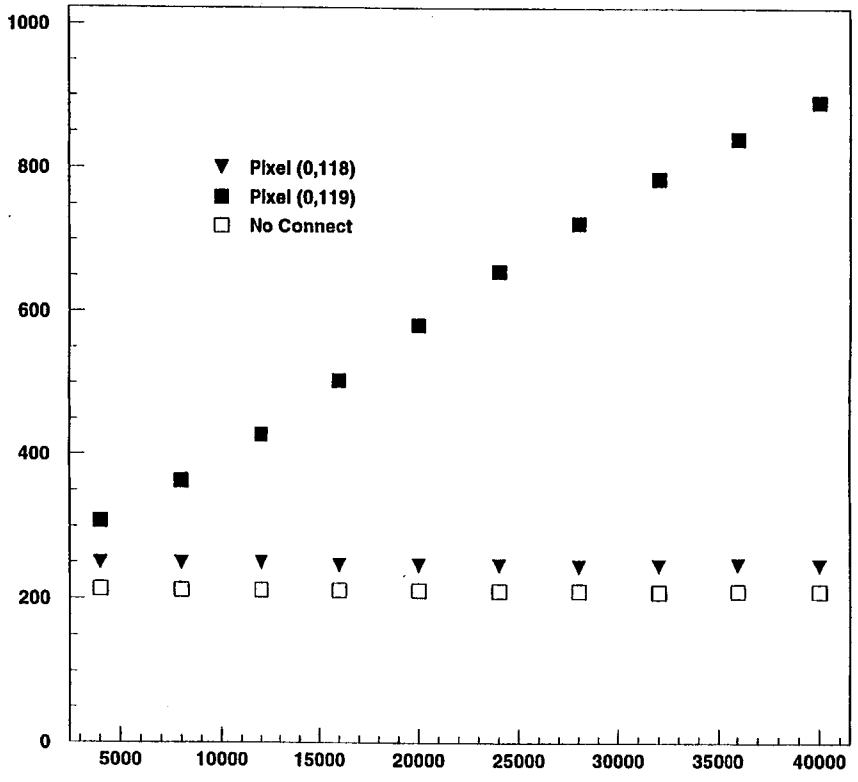

Macintosh
DAQ Hardware
Transceiver
Telescope Power
DAQ
BFE-A
BFE-B
BFE-C
Stage 3
M1
M2
M3
M4
Stage 2
Stage 1
Motor Driver
Master Control Board
S1
S2
S3
S4
Home Sensors
Efram Burlingame
6/6/97
4:35 p.m.
Telescope



G. Grim

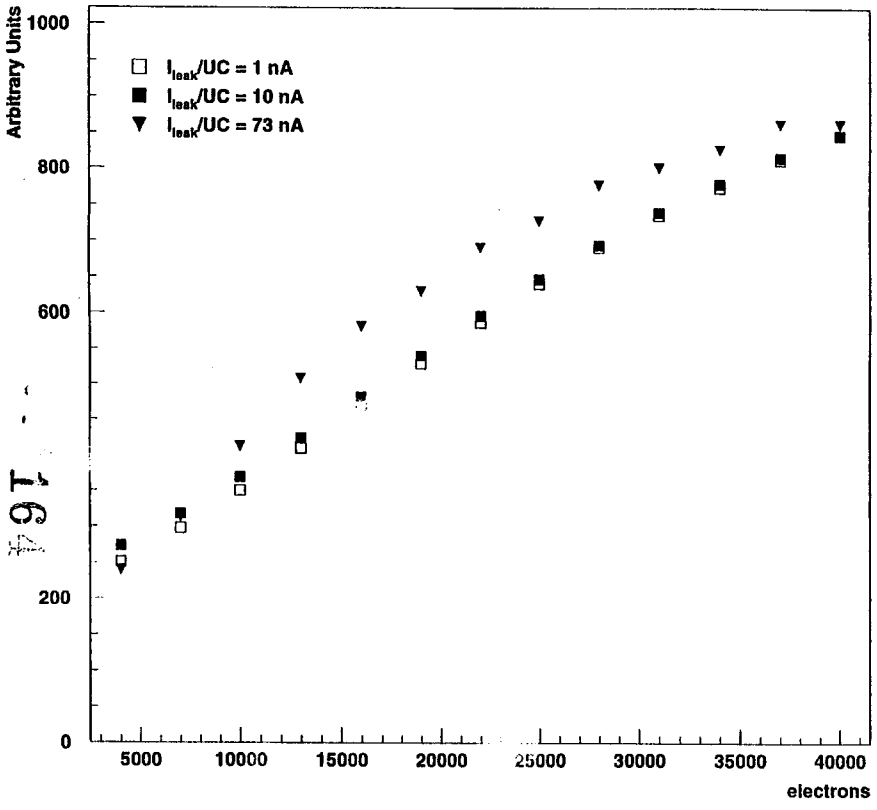
05/05/98 08.26

BFE-168 Performance



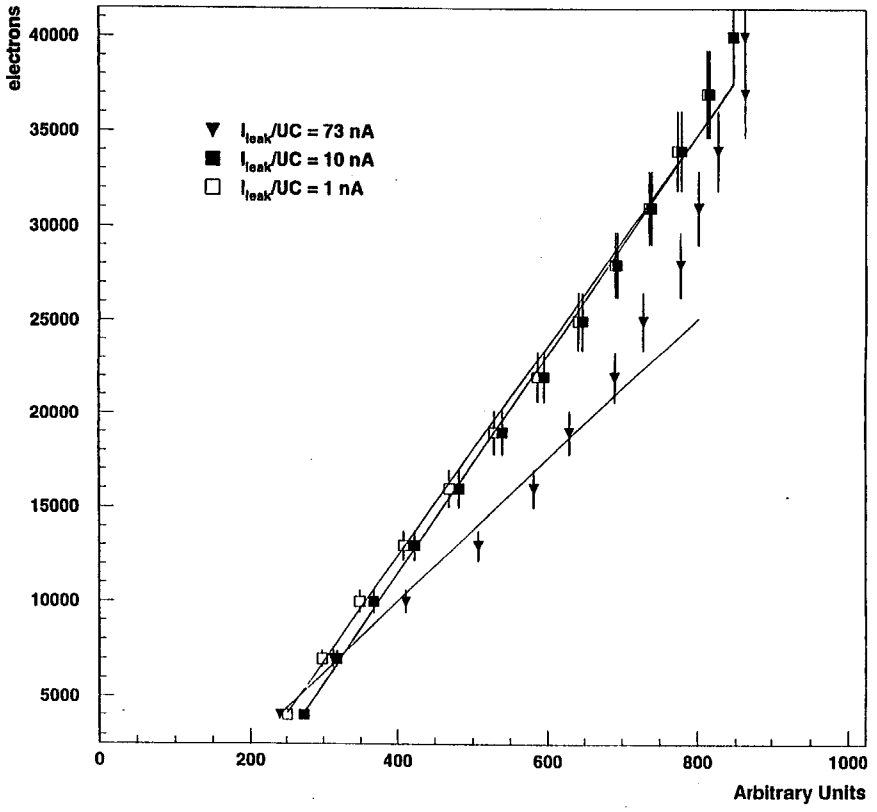
G. Grim 04/05/98 09.49

Leakage Compensation Performance



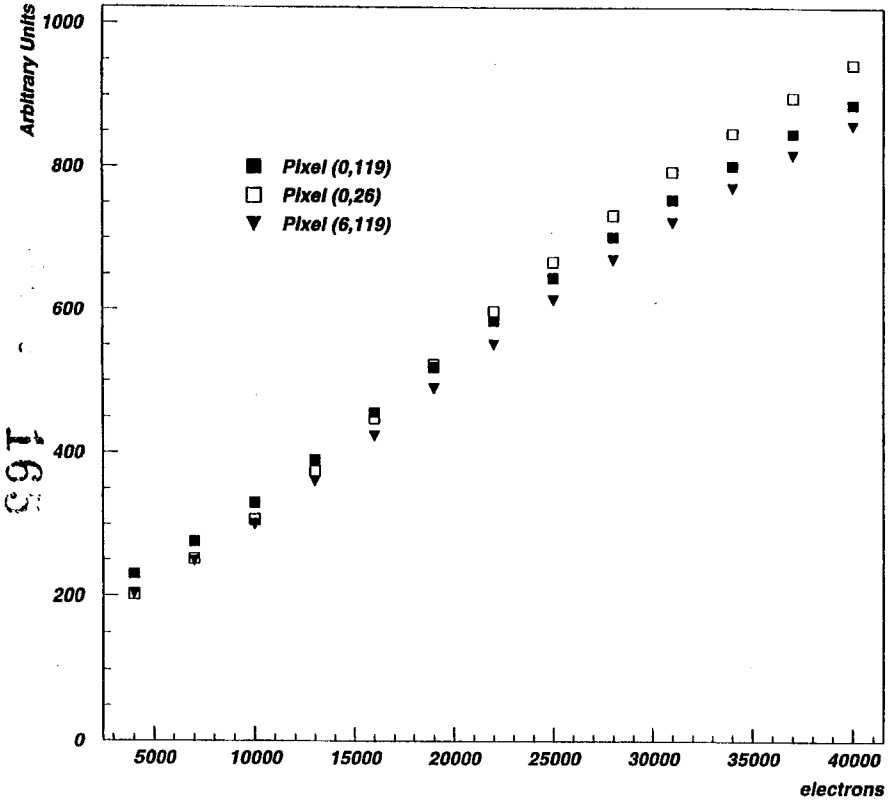
G. Grim 04/05/98 09.43

Leakage Compensation Performance



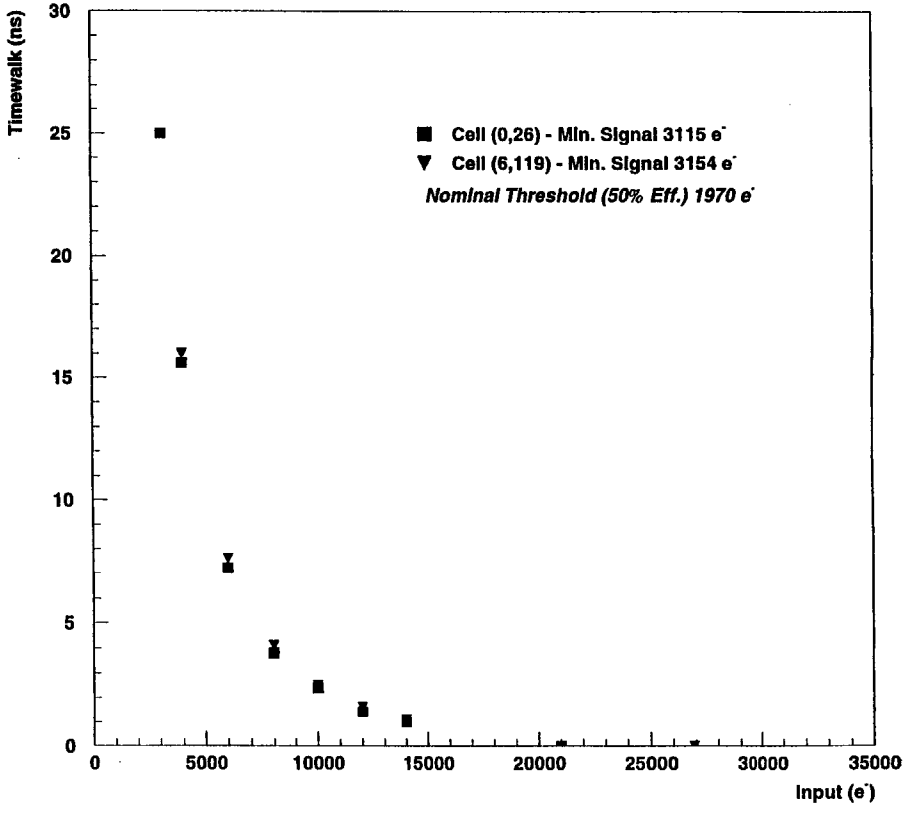
G. Grim 09/04/98 18.04

Chip-B3 UC Comparison



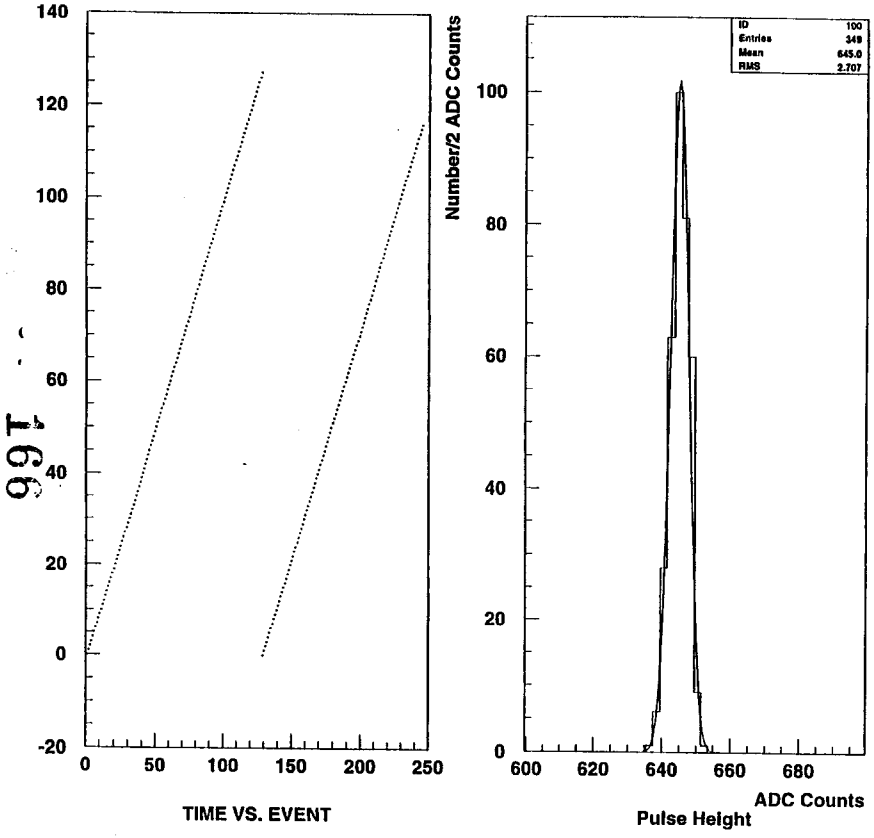
G. Grim 29/04/98 14.11

Chip-B3 UC Timewalk Comparison



05/05/98 08.12

BFE-168 Performance



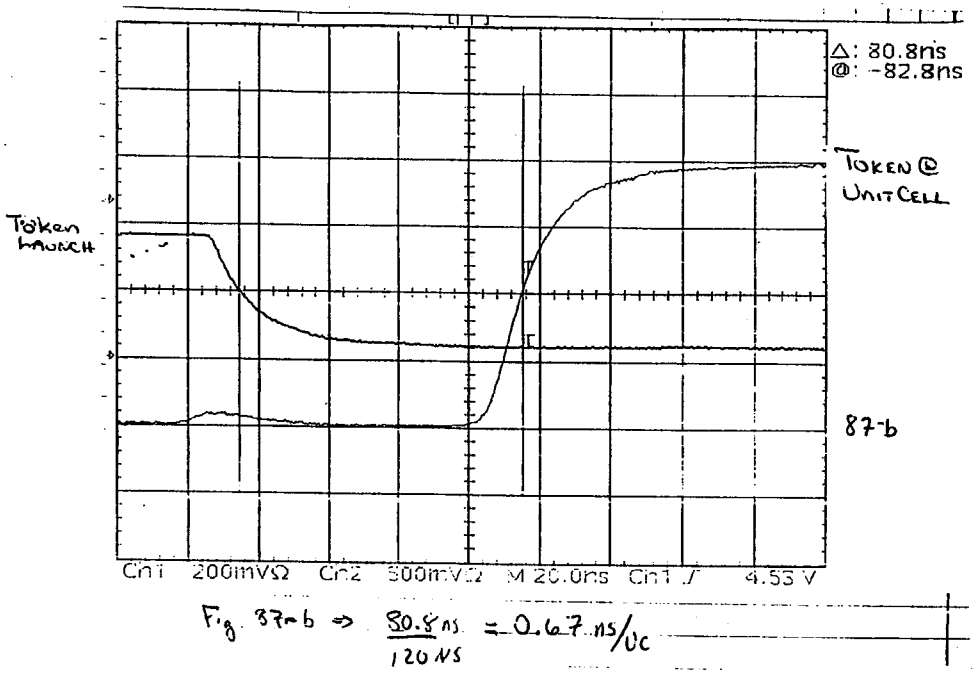


Fig. 87-b ⇒ $\frac{80.8\,ns}{120\,ns} = 0.67\,ns/Uc$

Re-verified Analog Front-End Performance.

- Original Results Presented @ Hungary 1996
- Linearity Good Enough - Spec.
- Timewalk 16 ns @ 4k electrons. - Spec.
  - Dual Comparator Coincidence
- Noise of 150 e^-'s RMS ENC - Spec.

Summary of Results

- Reverified Analog-Front End Performance.
- Power Consumption
- Leakage Current Capacity
- Column Readout Design

Leakage Current Capacity

- Max. Current 73 nA/UC
- Specification of 100 nA, Goal 150 nA
- From n+/p/p+ work, observe 7 pA/μm^2 @ Room Temp.
- For 150 μm x 150 μm UC @ 0 C => 10 nA/UC Avg.

Power Consumption

	Supply (V)	*Current (mA)*	*Power (mW)*	*Power/UC (μW)*
Vdd	3.00	3.75	11.25	11.7
VddA	2.50	3.12	7.82	8.1
VddP	1.08	12.18	13.15	13.7
Total	-	-	32.20	33.6

- Power Consumption per Unit Cell in Spec!

Column Readout Functions

- Basic Design Works!
- Token Speed ~1.5 GHz (Spec. 3 GHz)
- Pixel Mask & Neighbor Logic Works
- End of Column Time Stamp Works
- Bus Speed Needs Verification

Next Step

- Conversion to Honeywell SOI
- Rad-Hard to CMS Fluences - Dave Pellett Talk
- Simulation & Layout Conversion Complete
- Submission March 1998

K. Gabathuler, PSI

CMS PIXEL READOUT ELECTRONICS

PSI - ETHZ - Aachen
P. Dick, R. Horisberger, V. Karpinski, M. Lechner, G. Pierschel, R. Schnyder

Strategy:

- Test circuits are designed in radiation hard technology in order to keep control of the area finally required for a pixel unit cell and to monitor the performance before and after irradiation.
- Before going to the complex design of a large array chip, design the most critical elements of the circuitry. Their performance determine the final concept of the readout.

Design constraints:

- 4 Tesla field offers the use of large charge sharing effect for n-pixels.
- Square pixel size of 150 µm x 150 µm implies small pixel capacitance (≤100fF).
- Depletion depth of sensor > 200 µm up to 6 x 10^{14}/cm^2.
- MIP signal >12000 electrons up to 6 x 10^{14}/cm^2.

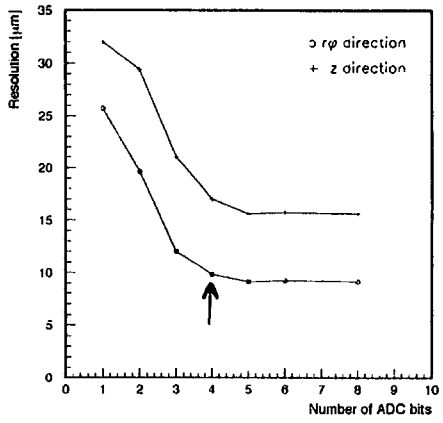
Design goals:

- Want to run with threshold of 2500 e up to 6 x 10^{14}/cm^2.
- With threshold at 5 σ noise, noise level must be below 500 e up to 6 x 10^{14}/cm^2.
- Data loss due to readout should not exceed ~1%.
- Power dissipated in readout chip should not exceed 60 µW per pixel.

CMS PIXEL READOUT ELECTRONICS

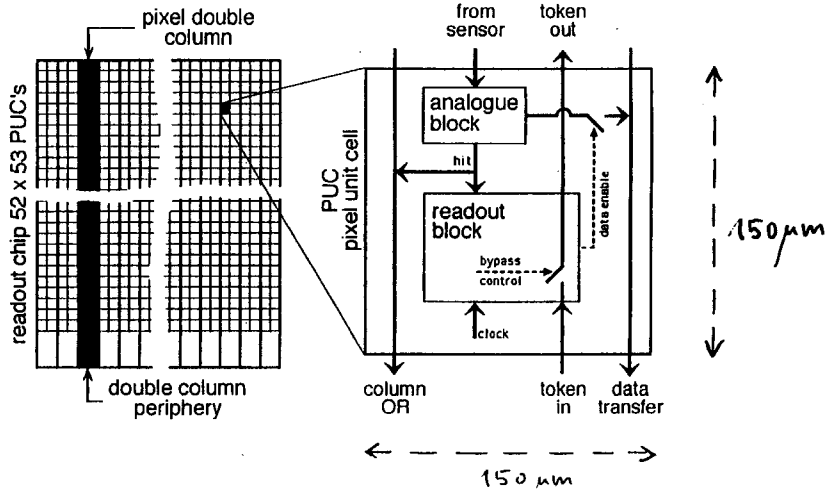
Main Features:

- Analogue Readout

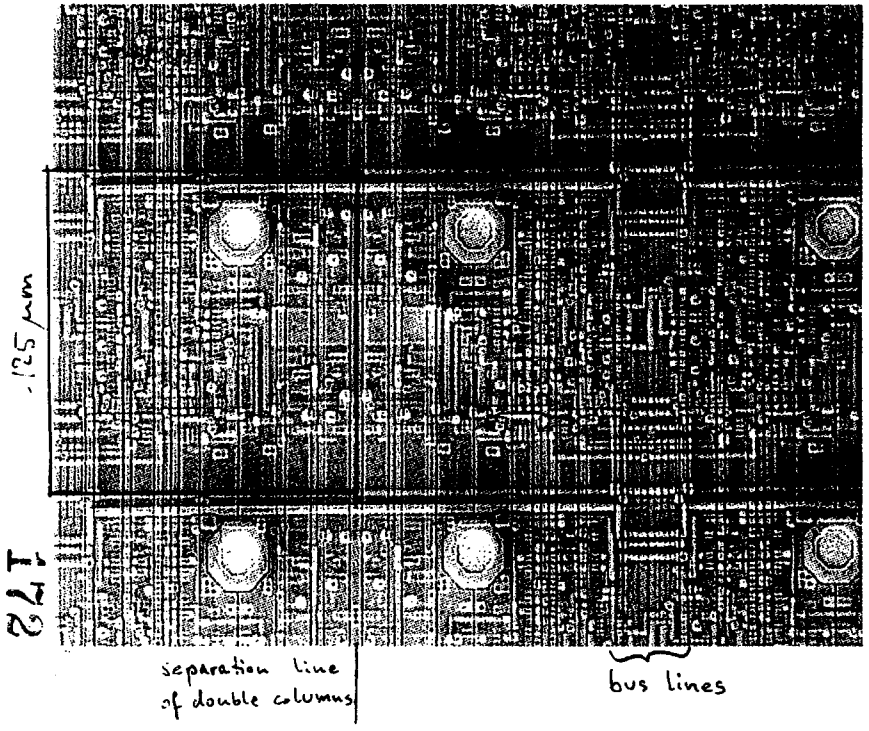


- Octal coded addressing

- Column based architecture (double columns)



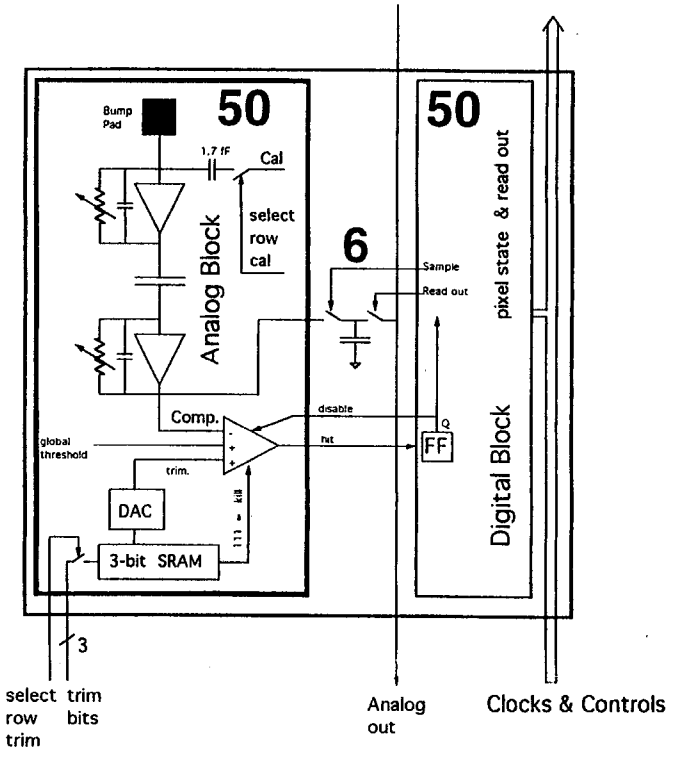
- Mirrored double column layout



- Column Drain Architecture
  Fast scan of hit pixels in a hit double column. Copy hits rapidly to periphery where they are stored for LT1 confirmation.

- Direct transfer of confirmed data from column periphery to counting room.

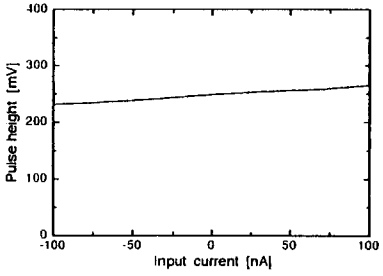
Analogue Block



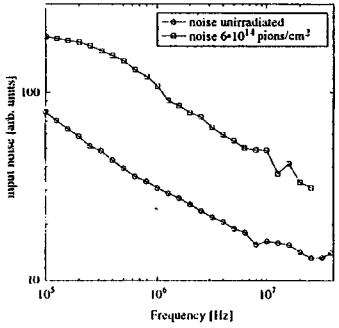
# of transistors

- Preamplifier&Shaper configuration
- Preamplifier feedback capacitance ~30 fF
- Preamplifier absorbs leakage current
- 20 - 30 e/mV at shaper output
- Common threshold for all pixels on chip
- Individual 3-bit threshold trim (111=kill)
- Column and row addressing scheme for trim bit programming and for applying selective calibration pulses
- Comparator disabled after hit

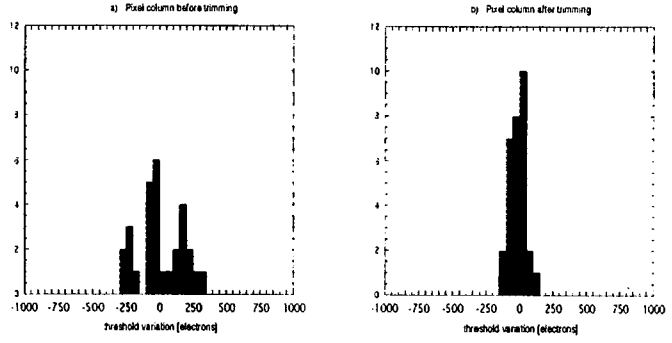
DMILL TEST CHIPS FOR ANALOGUE BLOCK



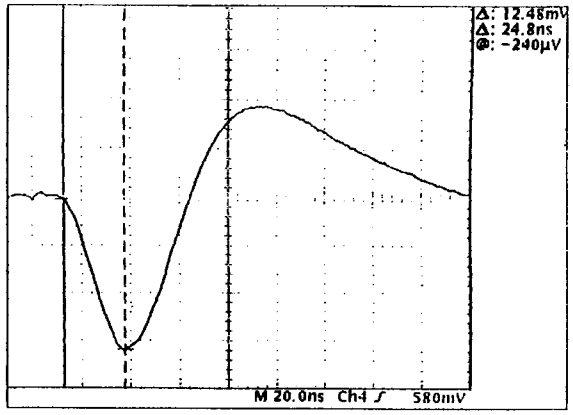
Signal variation at shaper output versus leakage current absorbed in preamplifier



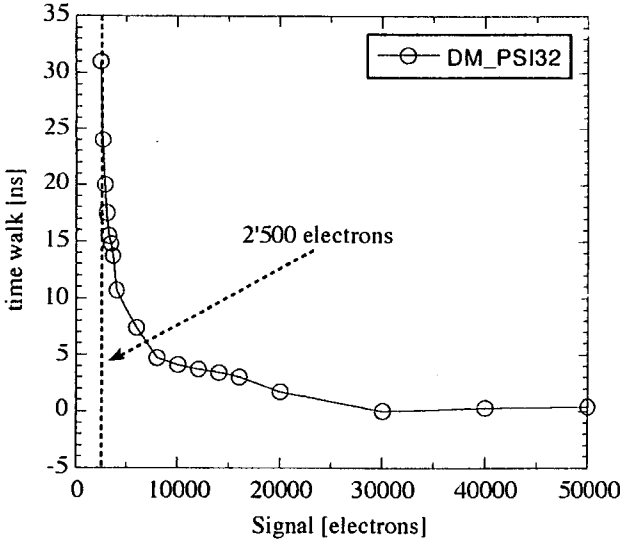
Noise increase of factor 3 after irradiation. Measured with input node capacitance of 160 fF, gives 650 e after irradiation. For anticipated 100 fF, noise expected 400 e after irradiation.

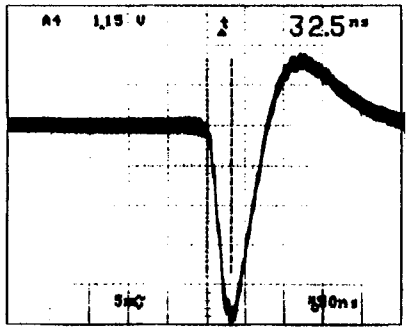


Pixel threshold distribution before and after trimming (unirradiated). Threshold ~ 1900 e, but can operate chip as low as 700 e threshold.

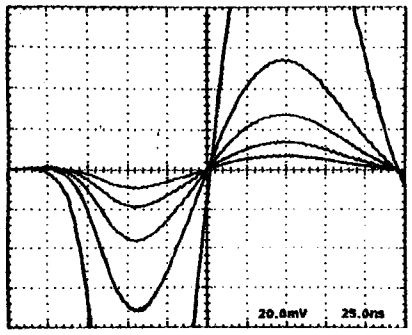


DM_PSI32, unirradiated.
Analog power ~40 µW.
Peaking time 24.8 ns.

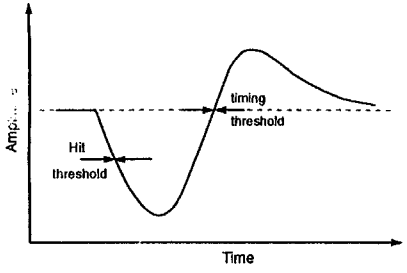


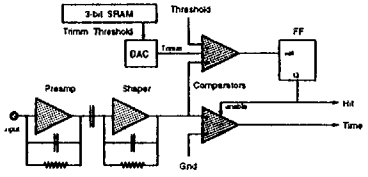


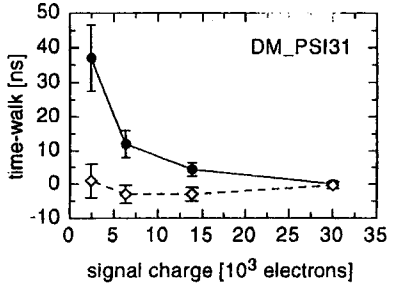
DM_PSI30, unirradiated
Peaking time 32.5 ns



DM_PSI26, irradiated with 10^{14}







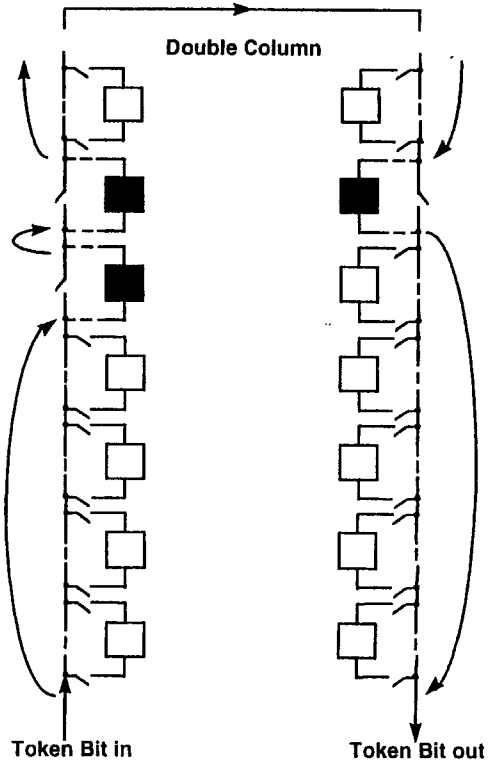
DM_PSI31, unirradiated

Zero Crossing Method

Must be checked after irradiation.

COLUMN DRAIN ARCHITECTURE

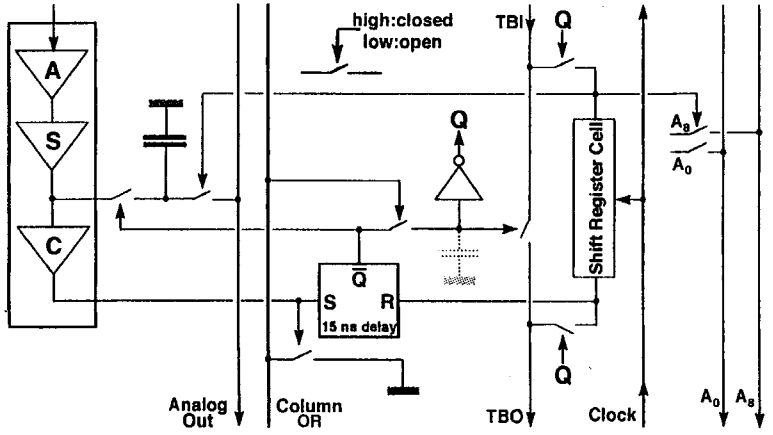
Upon a hit indicated via column OR to the column periphery, it sends a Token Bit through the column, skipping unhit pixels and stopping at hit pixels, initiating data drain to the periphery.



Travel of Token Bit up and down the double column takes about 8 b.c.

During this time more hits in so far unhit pixels in the double column from one additional b.c. must be allowed in order to reduce dead time.

CMS PIXEL UNIT CELL

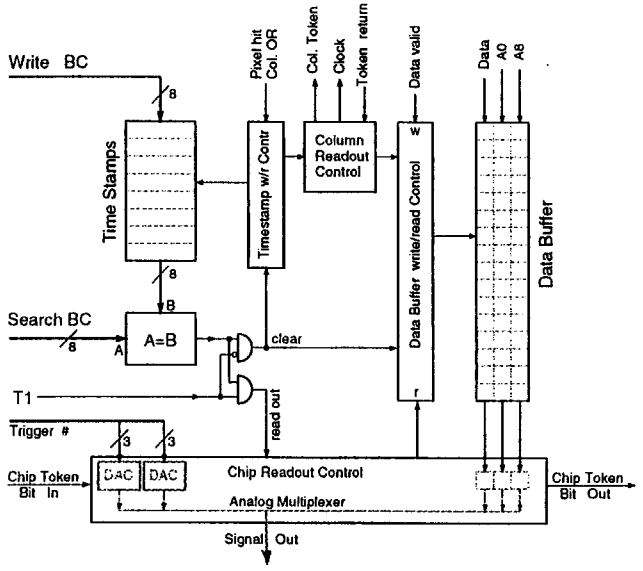


Any pixel in the column can pull the Column OR line to *LOW,* initiating a time stamp record in the column periphery . Upon sending a Token Bit on its way the column periphery resets the Column OR to *HIGH.*

The route of the Token Bit (*TBI* - TBO) is therefore only established when the Token Bit starts its travel through the double column.

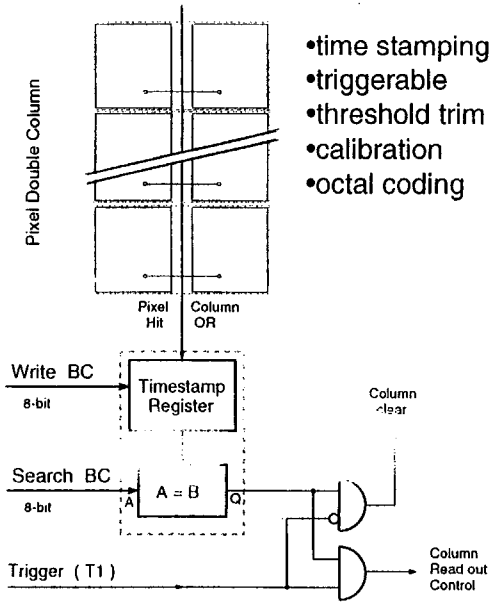
During Token Bit scan # n *one* additional time stamp can be recorded and its associated hits are drained with Token Bit scan # (n+1), during which time stamp # (n+2) is allowed, and so on (double buffering).

CMS PIXEL COLUMN PERIPHERY

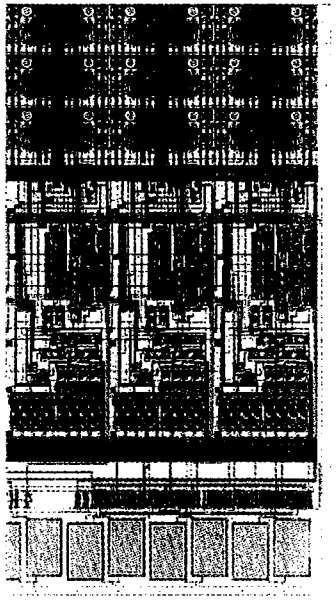


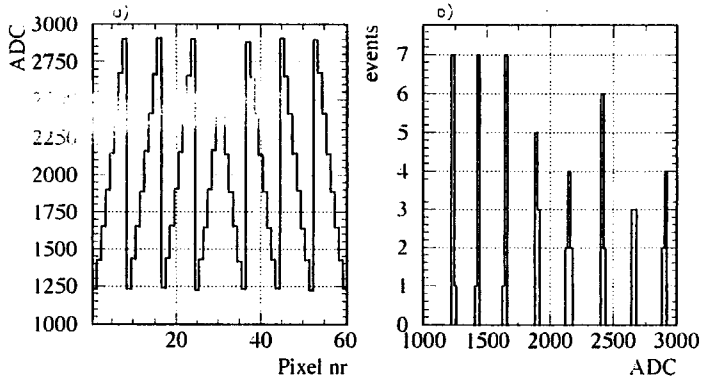
- Content of 8-bit local bunch crossing counter present in each periphery (*Write BC*). Ditto for *Search BC* which lags behind *Write BC* by 128 (1st level trigger latency)
- 8 *time stamp* registers (8-bit) organised in variable length FIFO.
- 24 data buffer cells of 3 switched capacitors. Variable association of data buffer cells to time stamp registers.
- Hand shake mechanism for Token Bit.
- Upon (*A=B and T1*) 6-bit trigger number is latched into two *DAC's* for octal coding.
- *Chip Token Bit* sent by Token Bit Manager Chip enables octal coded trigger number, pixel addresses and signal to leave the chip as a sequential analogue signal stream.

22 x 30 PIXEL CHIP



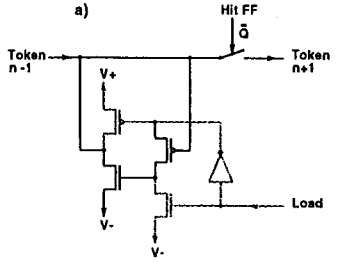
- time stamping
- triggerable
- threshold trim
- calibration
- octal coding

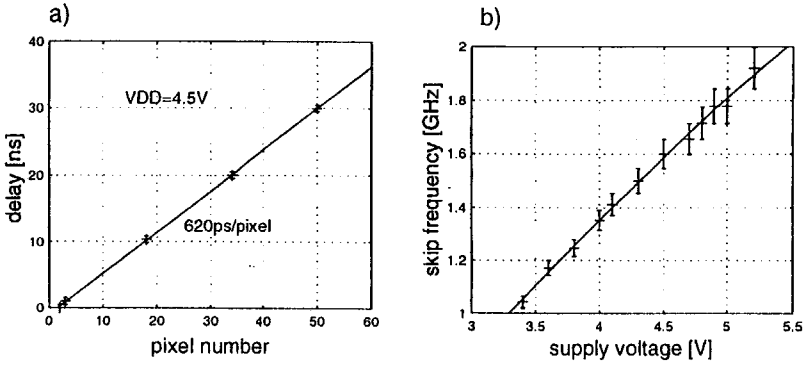




Lowest octal coded bit of pixel address for 30 pixels of one double column. (chip unirradiated)

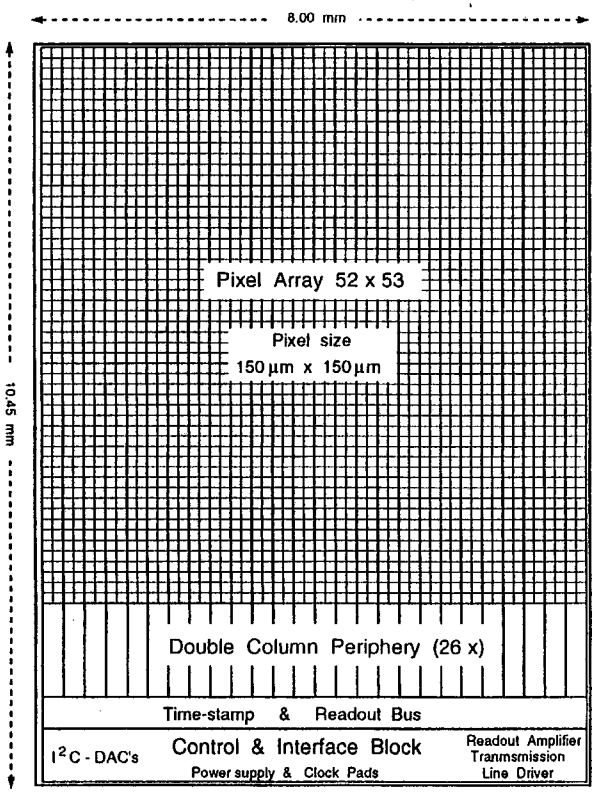
TOKEN BIT SCAN





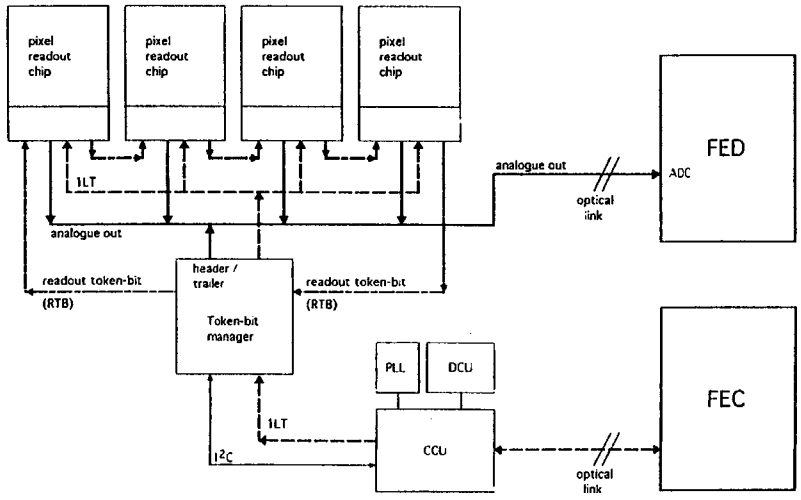
Token Bit takes 66 ns to travel through empty double column.

Crosstalk from Token Bit travelling through pixel to pixel input pad <750 electrons.



~ 380'000 transistors

READOUT OF TRIGGERED DATA



Token Bit Manager Chip

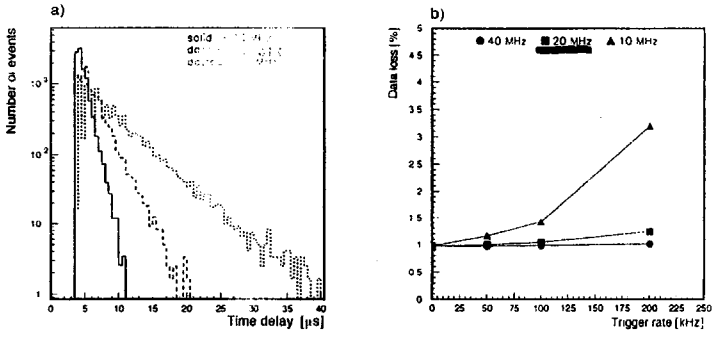
- Distributes clock and trigger signals to a group of chips.
- Manages a trigger signal stack.
- Puts data header/trailer onto the analogue out line.
- Sends Readout Token Bit according to content of trigger stack.
- Error handling and reset capabilities.

One readout frame has mixed data from different time stamps

Data Format

Data of one pixel hit	# of octal bits
Time stamp	2
Chip number	1
Column number	2
Row number	2
Signal	1
Header/Trailer/Marks	~2
TOTAL	**~10**

Data Transmission



Pedestal Loss of 1% is due to various losses in the raw (pre-trigger) data.

Pixel Detector for B-factories

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Abstract

Prospects for pixel detector upgrades of current e^+e^- B factories are investigated. Relevant technologies are compared. The results of some preliminary simulations and fabrication R & D are presented.

1 Introduction

B-factories are the new generation of particle accelerators capable of producing copious numbers of B-mesons. B-mesons, being heavy, have hundreds of decay modes, and therefore create a large arena for the test and measurement of Standard Model. Out of many physics topics to be studied in B-factories, test of fundamental symmetries is perhaps the foremost. The product of charge conjugation and parity (CP), which was thought to be a fundamental symmetry of nature, was found to be violated in the decay of K-mesons. Even more than 30 years after this discovery, the phenomenon of CP violation has not been observed in any other system. The Standard model, on the other hand, does allow for CP violation through complex phases in the quark rotation matrix, called Cabbibo-Kobayashi- Masakawa(CKM) matrix, which along with the magnitudes of the matrix elements, are poorly determined parameters.

The major goal of the B-factories is to discover the phenomenon of CP violation in B-meson decays, measure the CKM parameters, and therefore check if the observed CP violation can be explained within the scope of the Standard Model. These experiments have the potential to answer the very fundamental question : why is the universe that we see today is made of mostly matter, with anti-matter only scarcely present ? Such a situation can occur if there is a large enough CP violation in the physical laws of nature.

Electrons and positrons can collide to produce a quark-antiquark pair. The largest cross-section for B-mesons (a "beauty" quark paired up with any other quark) occurs at the $\Upsilon(4S)$ resonance at a center-of-mass energy of 10.58 GeV. The B-factories at (1) Cornell University, CESR ring, CLEO detector, (2) Stanford Linear Accelerator Center, PEP-II ring, BaBar detector, (3) High Energy

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Talk presented at the Pixel 98 workshop at Fermilab during May 7-9, 1998.

Accelerator Physics Lab (KEK, Japan), KEK-B ring, BELLE detector; will all run at this energy. PEP-II and KEK-B will be asymmetric (different momenta for electron and positron beams), while CESR will be a symmetric accelerator. In Fig. 1 we show the geographic location of these B-factories and in the inset show their operating region in center of mass energy.

The decay vertices of the B-meson and its secondaries play an important role in the physics being pursued, and therefore much effort has gone into building silicon strip detectors for vertexing. Intrinsic position resolution of these detectors are typically about 5 - 15 microns, and the impact parameter resolution is typically 80 - 200 microns. For the initial discovery physics, this kind of sensitivity is enough, but as we proceed into the measurement and deeper disovery arena, much better vertexing is desirable. In Fig. 2 we show the decay lengths ($\beta\gamma c\tau$, with $\beta\gamma = 0.43$ for KEK-B) of some important particles generated at B-factories, compare them with resolutions of a common silicon strip vertex detector (SVD) and a novel silicon pixel detector (PIX) combined with the SVD. Clearly, the hybrid system (PIX+SVD) probes deep into the decay kinematics.

Both, silicon strip and pixel detectors are essentially reverse-biased PIN($p - intrinsic - n$-type) diodes. When a charged particle goes through, the ionization creates electron-hole pairs, which drift in opposite directions and create a signal when they strike the respective electrodes (see Fig 3). In the case of the strip detector, the electrodes look like strips running in orthogonal directions on p and n planes, and therefore the signal-bearing strips give the information on the position of the track. For instance, upper plane of the strip detector sketched in Fig. 3 gives the z-position measurement, and the bottom plane gives the y-position measurement. In the case of the pixel detector, however, since one of the electrodes is segmented into tiny rectangles, called pixels, both z and y measurements come from just the top plane.

2 Proposed Upgrade of SVD

In this paper, we will take the Belle detector at the KEK B-factory as a generic e^+e^- B-factory, and build our arguments around it. The same arguments can be extended to BaBar and CLEO with certain constraints.

Vertex resolution is dominated by two factors : geometry and multiple scattering. A pedagogical model with two layers of vertex detector (for the sake of simplicity) is shown in Fig. 4. The two detector planes are parallel to the beam, at radial distances r_1 and r_2. Intrinsic resolutions are σ_1 and σ_2, respectively. The goal is to make the impact parameter resolution σ_{d0} as small as possible. It comprises of two factors - geometric error (σ_{geom}) and multiple scattering error (σ_{ms}) :

$$\sigma_{d0}^2 = \sigma_{ms}^2 + \sigma_{geom}^2 \tag{1}$$

$$\sigma_{geom}^2 = \left(\frac{\sigma_1 r_2}{r_2 - r_1}\right)^2 + \left(\frac{\sigma_2 r_1}{r_2 - r_1}\right)^2 \tag{2}$$

$$\sigma_{ms}^2 = \Sigma_{j=1}^{ndet}(R_j \Delta\theta_j)^2 \tag{3}$$

$$\Delta\theta_j = \frac{0.0136}{p[GeV/c]}\sqrt{\frac{\Delta x_j}{X_0}}\left[1 + 0.038 \ln\frac{\Delta x_j}{X_0}\right] \tag{4}$$

where R_j is the radius of the inner detector(s) that need to be taken into account for estimating tracking error due to multiple scattering. It may be noted that these equations assume perpendicular incidence, and therefore a $\cos\theta$ factor enters in the denominator when slanted tracks are considered.

Examining the above equations we determine that for better vertexing :

1. r_1 and r_2 should be small, which means detectors should be as close to the interaction point as possible.

2. $(r_2 - r_1)$ should be as large as possible, which means the lever arm should be large.

3. $\frac{\Delta x_i}{X_0}$ should be small, in other words, the detector itself should be as thin as possible.

Keeping these factors in mind, we propose the following : (1) reduce the beampipe diameter (2) add two layers of *thin* pixel detector. The advantage of doing this has been simulated with a program called TRACKERR. The most relevant results are shown in Figs. 5 & 6, where the impact parameters $\sigma_{r\phi}$ and σ_z are plotted as functions of the dip angle of a 250 MeV incident pion. Intrinsic resolution of 10 μm is assumed for both, PIX and SVD detectors. The solid lines are for the SVD+PIX option with 100 μm pixel thickness, dashed lines are for the SVD+PIX option with 350 μm pixel thickness, and dotted lines are for the existing SVD only option. For the PIX option, it is assumed that one can reduce the beampipe radius to 1 cm, and that a 0.3% X_0 synchrotron/EM shield exists just outside of the beampipe.

The significant improvement in tracking and vertex resolution, especially at the low angle region is worth taking the trouble of putting a pixel detector in. Rigorous analysis on this topic may be found in [1].

In what areas do we expect physics gains ?

1. The $b \rightarrow s$ transitions, mediated by penguin diagrams are hard to separate from the $b \rightarrow c \rightarrow s$ backgrounds without good vertexing.

2. The $b \rightarrow u$ transition is a rare decay, and the matrix element V_{ub} is a poorly determined parameter. Measurement of this decay mode is made difficult by continuum background, which can be suppressed by good vertex separation.

3. Direct measurement of T-parity violation can be studied in polarization studies of $b \rightarrow c\tau\nu$. Detection and polarization measurements are difficult without excellent vertex detection.

In general, any process with a secondary vertex or where either combinatoric background is large or continuum background is large, will be easier to study with a pixel detector.

As a generic B-factory detector, we use the Belle detector at KEK B-factory to establish our point. In Fig. 7(a) cross-sectional view of the current Belle vertex detector is shown. It consists of three layers of silicon strip detectors with a 2 cm radius beam-pipe. We propose to reduce the beam pipe radius to 1 cm, and put two thin pixel layers at 1.3 and 2 cm. The resulting arrangement is shown in Fig. 8. The $r\phi$ view is given in Fig. 9. The hexagonal shape for both the layers ensures ease of mechanical fabrication, but leaves some dead space at the corners. An alternate design, shown in Fig. 10 has a hexagon-octagon shape. This has the advantage that sensors of the same size for both the pixel layers can be manufactured, thus making the yield higher.

3 Radiation Damage

Radiation damage in the B-factories is dominated by $e^{\pm}\gamma$ background from synchrotron radiation and beam-gas scattered electrons (hereafter referred to as *spent electrons*). Damage to the detector and circuit is mainly due to ionization. This differs from the type of damage at LHC, which is mostly field and gate oxide damage, as well as bulk damage due to proton, neutron or pion irradiation.

Synchrotron background is a characteristic of the machine, and the problem is different for each B-factory. In Fig. 11 we show the synchrotron radiation fans at BaBar and Belle detectors. At BaBar, the fan hits the detector region directly, and hence sophisticated masking is necessary. In Belle, the dotted lines show the 10σ synchrotron profile, and it stays clear of the detector/beampipe. Hence the beampipe radius can be reduced without being directly hit by the synchrotron radiation. In any case, we assume that synchrotron radiation can be masked, and that the majority of damage will come from spent electrons.

Spent electrons (or positrons; we will call them spent electrons in a collective sense) are produced when the beam electron scatters off a residual gas nucleus via Coulomb scattering or Bremsstrahlung. The spent particle changes direction or energy, and goes off the orbit. The new trajectory, after passing through a number of electromagnetic elements in the accelerator may hit the detector, and thus produce hits and radiation damage. Simulations of such backgrounds have been performed at all the three B-factories, and details of the results may be found in the proceedings of the First and Second Workshops on Backgrounds at Machine-Detector Interface([2]). For Belle, the results are summarized in Fig. 12, where expected the dose is plotted as a function of the radial distance from the beamline. The position where the pixel detector will be gets upto a MRad of dose per year, which would be too much for conventional strip detectors and associated electronics. Although the electronics could be made rad-hard, the large capacitance and large leakage current of strip detectors would render them inoperable at such high doses. Again, the occupancy would be too high for a strip detector.

Getting the detector and the electronics rad-hard upto at least 5 MRad is conceivable with current technology, thanks to success in development of radhard electronics for LHC.

It is worthwhile to mention that the backgrounds are a strong function of the beam emittance. A representative diagram of beam emittances at PEP-II, CESR and KEK-B is given in Fig. 13. The very low emittance at KEK-B makes it a lot easier to put a pixel detector close to the beam.

4 Possible Options

The B-factories will start their runs in early 1999. We plan to install the pixel upgrade after two years of initial running, which means we have to make a working detector by the end of the year 2000. Keeping this goal in mind, we have evaluated several options for vertexing technology.

- **Diamond Pixels :** It would be the best detector option, given its radiation hardness. But the technology is currently being developed, and there aren't multiple vendors of the detector grade material to ensure uninterrupted supply. This option would be too risky for this project.
- **Thin Silicon Strips :** These are a possible option, although signal to noise is a problem. Some groups have produced such detectors with partial success. Advantage is that one can use commercially available Viking VH1 radhard chips with these detectors. This is a potential *intermediate* upgrade option.
- **Thin CCDs :** CCDs have been used in HEP experiments and backthinned CCDs can be presumably used for this purpose. But the charge transfer (shift register) mechanism limits the capability of operating the detector at high background rates. The signal would be swamped in backgrounds during charge transfer.
- **Thin Silicon Pixels (bump-bonded) :** This is a potential option for us, and the rest of the paper is written taking this as the default. By choosing this, we are flying on the wings of ATLAS/CMS expertise.

- **Thin Silicon Pixels (Monolithic) :** With lower capacitance than bump-bonded ones, these have better S/N performance. This could be a potential option if the technology can be made rad-hard. This option is still under study.

- **Thin Slicon Pixels (3D) :** This is a novel innovation in silicon detector technology. But it is in the process of being developed, and would clearly be too ambitious for this project.

We are currently carrying out R & D for the bump-bonded thin silicon pixel option.

The proposed manufacturing process of the detector is described in Fig. 14. One starts with a 500 μm readout wafer and a 70 - 100 μm detector wafer. The detector is then backed up with wax by a 300 μm dummy wafer. Indium bumps are deposited on both sides, and pressure bonding is performed. The sandwich is cut with diamond saws to the desired size, and by dissolving the wax the dummy support is removed. The readout wafer is then back-thinned by cold reactive plasma etching down to 50 μm or less. One is then left with a complete thin detector ready to be installed.

In the Belle detector, the acceptance is from 17° to 150°, and therefore the rule $L = 5R$, where R is the radial distance of the detector from the beamline and L is the minimum physical length of the detector, applies (see Fig. 15). Since we want to put the detectors very close to the beamline, with R less than 2 cm, a whole sensor can be comfortably carved out of a 4 inch or at worst 6 inch wafer, both of which are standard. Such a "one-piece" detector eliminates the need of inter-sensor wire bonding, and simplifies the structural issues greatly.

5 Some Rules of Thumb and "a" Readout Architecture

The pixel upgrade we propose need not have any time-stamp information, since the trigger will be provided by the silicon strip and TOF detectors. With only charge information needed, the number of transistors, capacitors and resistors will be small, and therefore the size of the pixel can be made small. We envision a 50 $\times$ 50 μm^2 pixel size. Bump bonds are reliably done at diameters of 20 μm or large, and could comfortably fit into this pixel dimension. With 100 μm thick detector, the number of e-h pairs produced per MIP will be about 8000. In order to get good position resolution, the readout has to be analog and we need to get the charge sharing information from neighboring pixels. Assuming a 3×3 pixel clustering scheme, we should be sensitive up to about 20% of the total charge, which corresponds to 1600 electrons. Using the canonical S/N = 10/1, we get 160 electrons as the ENC of our electronics, which is achievable with current CMOS technology.

The readout/Integration time and dynamic range of the electronics depends on the degradation of the detector and electronics due to radiation. A useful parameter is the dark current. A good detector will have a dark current of the order of 10 nA/cm^2. A few MRad of dose will increase it to about 50 nA/cm^2. On a 50 $\times$ 50 μm^2 size pixel, this corresponds to 0.25 pA - 1.25 pA of dark current. With the 160 ENC number discussed in the last paragraph, the time becomes 160 e^-/ 1.25pA = 20 μsec. This means the integration time can be as long as 20 μsec even though the beam crossing is only every few nano seconds.

Since the physics event rate is less than 10 kHz and the event multiplicity is less than 8 for B-factories, the above scheme should work well.

A simple proposed architecture for readout is shown in Fig. 16. It is a modified version of an original design by Aw, Kenney and Parker. One sensor module consists of typically 2000 rows and 200 columns. When a row is hit and the charge collected is larger than the threshold, then the address of that row is encoded. During each scan cycle, the control loops over the encoded rows, and strobes all the columns of that row to be read out in parallel. These 200 signals can then be

digitized, and may be filtered and/or delayed through an SCA/FPGA for a quick quality scan before being dumped into the database. Some multiplexing and zero-suppression may be required at this step if the power consumption becomes too large. All the analyses can be done offline.

6 Experience with Thin Wafers

At the Center for Integrated Systems(CIS), Stanford and the Fabrication Lab at UC, Davis we have done some rudimentary work on thin wafers. Starting from 300 μm, wafers have been thinned down to 70 μm by chemical etching. Processes such as dump rinsing, spin rinsing, spin resist, lithography, wet oxidation and dicing have been tested with good yield. Cold reactive plasma etching has been done without doing any visible damage to bumpbonds. Processes such as metallization and bump bonding will be tested on these thin wafers in near future.

In Fig. 17 we show a picture of lithography done on a thin wafer. The structures visible are about 20 μm wide. In Fig. 18 we show the cross-section of a diced thin wafer, still supported by the dummy wafer with wax.

7 Future Directions

The following goals are set for the installation of a pixel detector at the KEK B-factory. These are highly contingent upon manpower and financial resources.

- All processing techniques for thin wafers will be established this year (1998). The production will either be done by ourselves or vended to any interested manufacturer with the technology transfer.
- A diode prototype will be made by the end of 1998.
- Charge drift simulation for thin pixels and device optimization for readout will be done by the spring/summer 1999.
- A readout chip will be fabricated by mid 1999.
- A full prototype will be ready by the end of 1999.
- Assuming the backgrounds permit, a full detector will be made in 2000 and installed at the end of the year.

Acknowledgement

References

[1] "Track Origin Reconstruction Resolution with a future Belle Pixel Detector", T.E. Browder *et al.*, To be published as a Belle Note (http://bsunsrv1.kek.jp).

[2] Proceedings of the First and Second Workshops on Backgrounds at the Machine Detector Interface, Hawaii 1995 (Ed. T.E. Browder, UH-511-838-96, available from www.phys.hawaii.edu/~beam/proceedings.html), 1997 (Ed. T.E. Browder and S.K. Sahu, in print at World Scientific, partial contributions available from www.phys.hawaii.edu/~beam/papers.html)

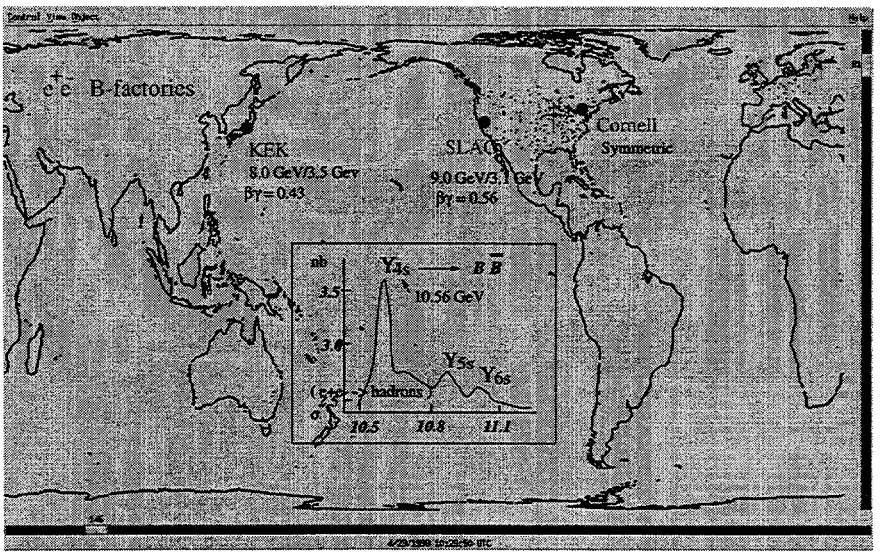

Figure 1: Geographical location of the e^+e^- B-factories. The inset shows the operating energy at $\Upsilon(4S)$ resonance.

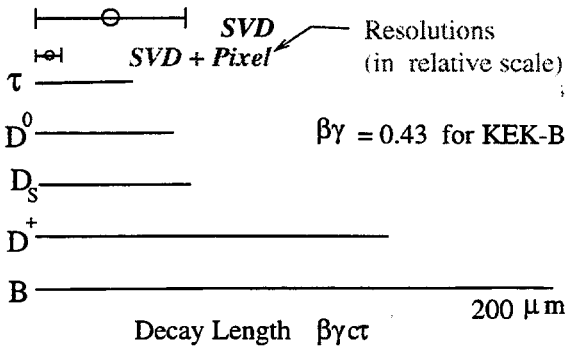

Figure 2: Decay lengths of some particles in relative scale, compared with resolutions offered by SVD and SVD+Pixel. Both SVD and PIX are assumed to have intrinsic resolution of 10 μm. SVD has 350 μm wafers, and PIX has 100 μm wafers. SVD option assumes a 2 cm radius beampipe, whereas the SVD+PIX option assumes a 1 cm beampipe.

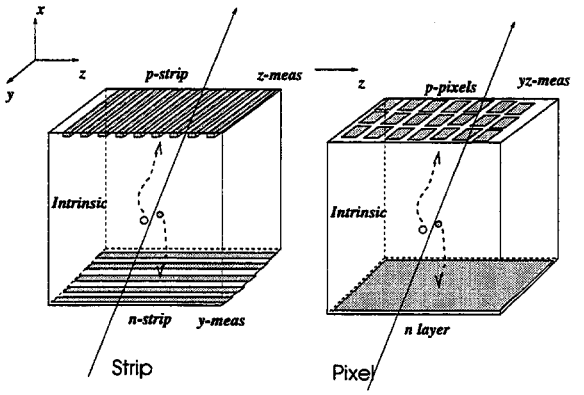

Figure 3: Conceptual comparison between silicon strip detectors and silicon pixel detectors. The arrow represents a charged particle, and the two circles represent an electron-hole pair out of thousands created. The electron drifts to the n-side (the detector is always reverse biased), and the holes drift to the p-side, generating a signal current upon arrival.

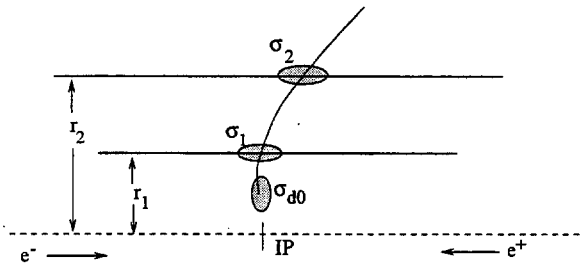

Figure 4: Model of a two-layer vertex detector.

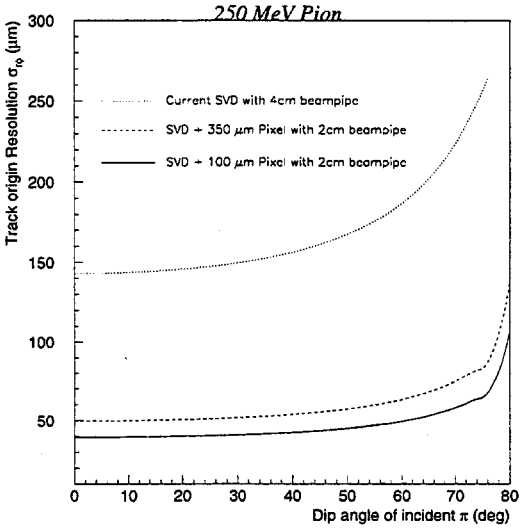

Figure 5: Impact parameter resolution in $r\phi$ plane as a function of dip angle for pions of different momenta.

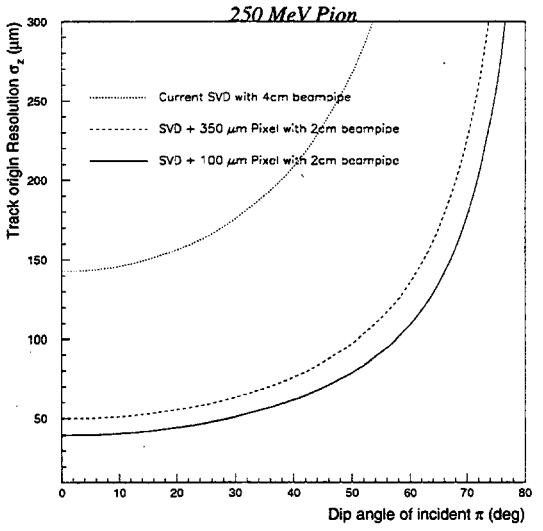

Figure 6: Impact parameter resolution in z direction as a function of dip angle for pions of different momenta.

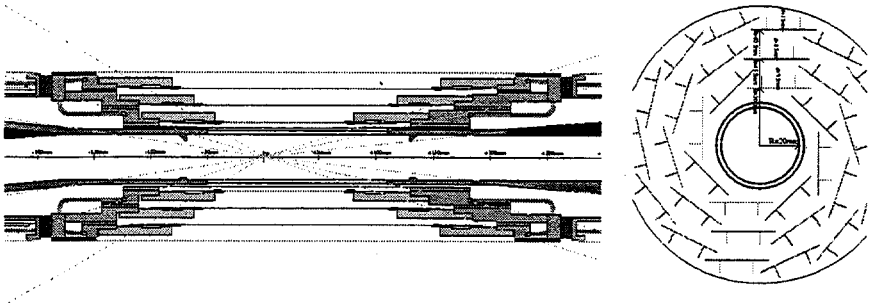

Figure 7: xz and $r\phi$ views of the current Belle silicon vertex detector (SVD).

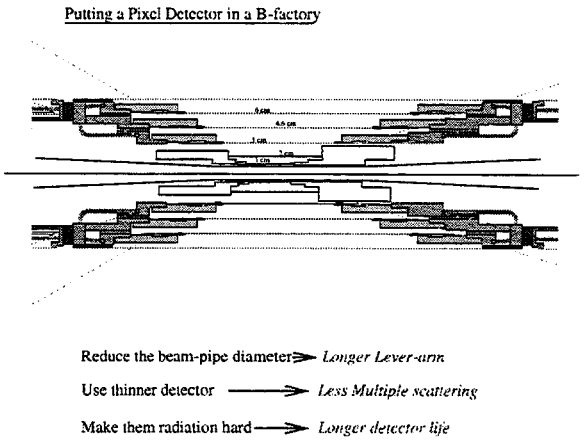

Figure 8: xz view of the proposed pixel detector upgrade at Belle.

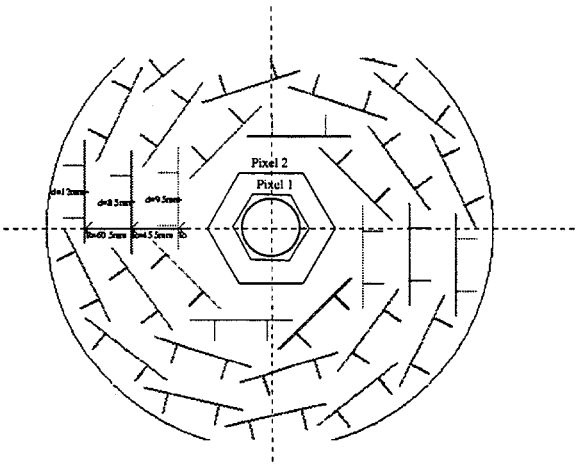

Figure 9: $r\phi$ view of the proposed pixel detector upgrade at Belle.

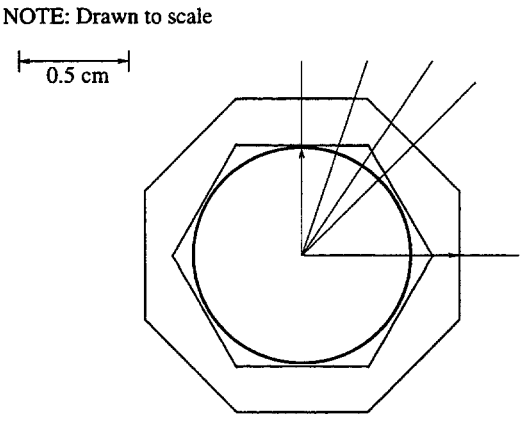

Figure 10: $r\phi$ view of another option for a pixel detector upgrade at Belle.

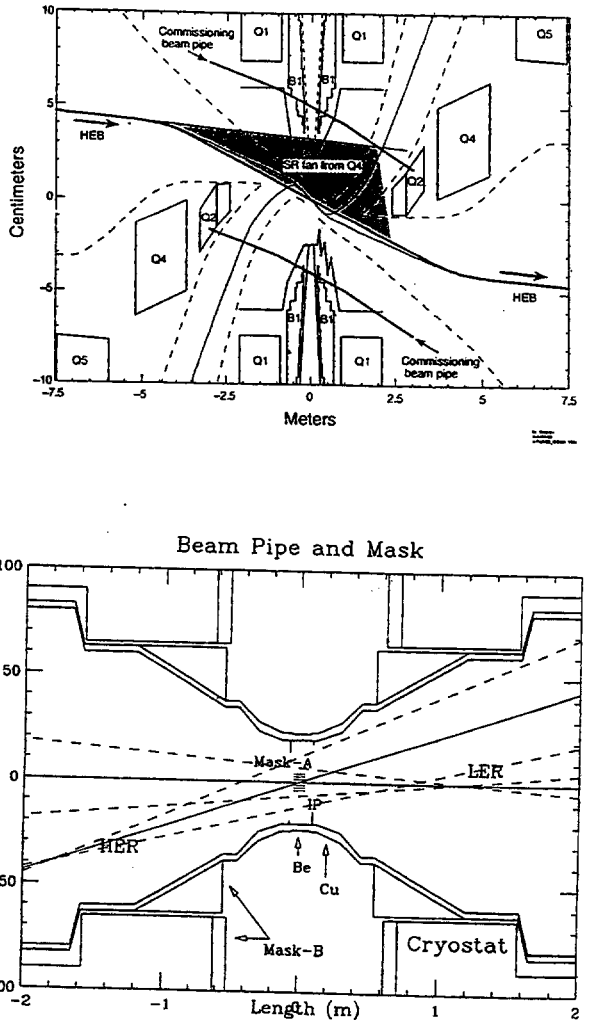

Figure 11: Synchrotron radiation fans at BaBar (top) and Belle (bottom). Dotted lines for Belle represent 10σ contours.

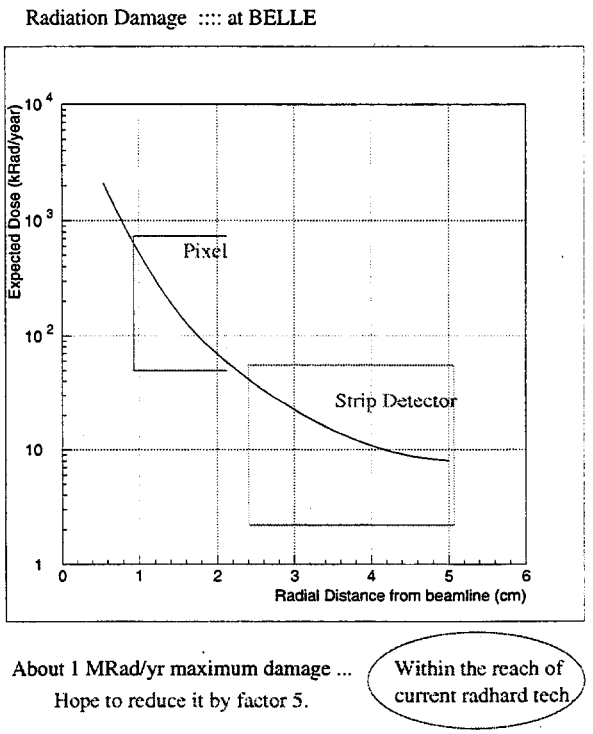

Figure 12: Radiation dose as a function of radial distance due to spent electrons at Belle.

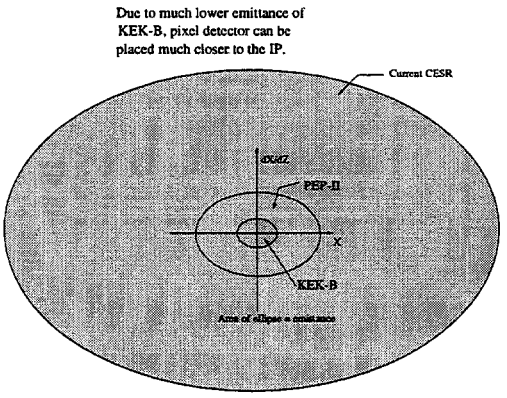

Figure 13: Beam emittance in the three B-factories in a relative scale. The area of the ellipse is a measure of the emittance.

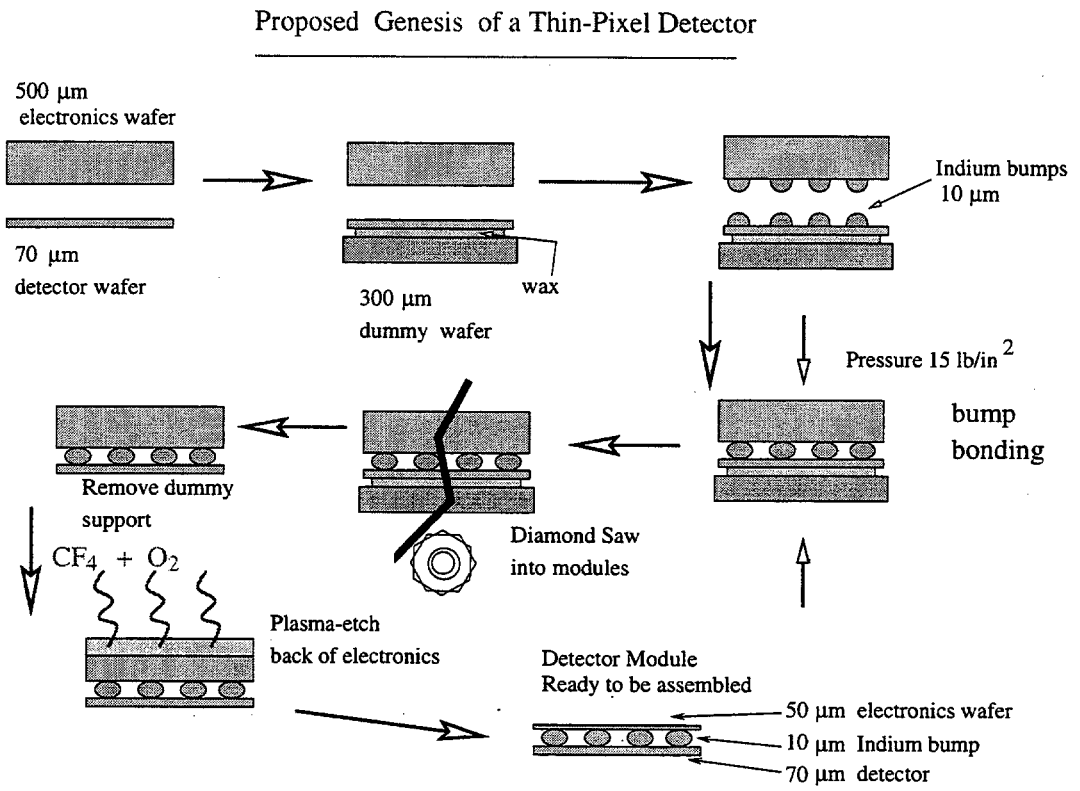

Figure 14: Proposed production process of a thin bump bonded pixel detector.

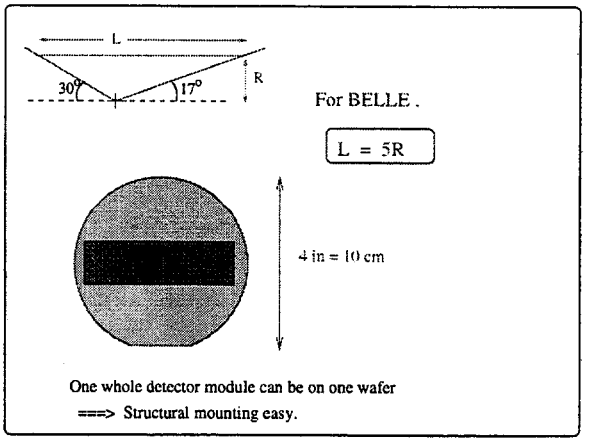

Figure 15: At small radii, the whole pixel sensor can be accomodated on a single wafer : the $L = 5 \times R$ rule.

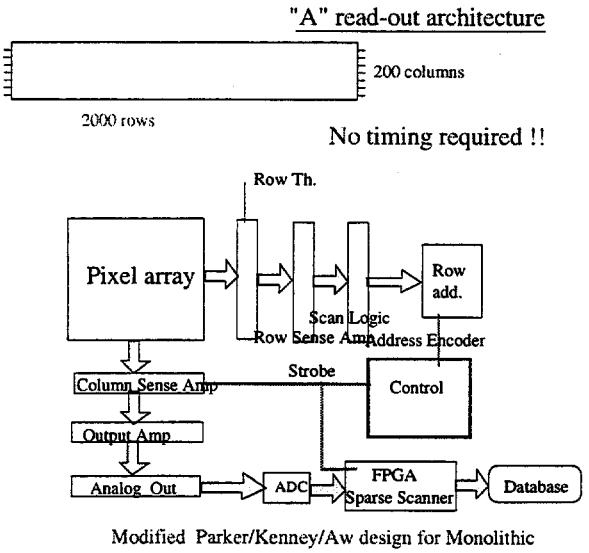

Figure 16: A simple proposed readout architecture for B-factory bump-bonded pixels.

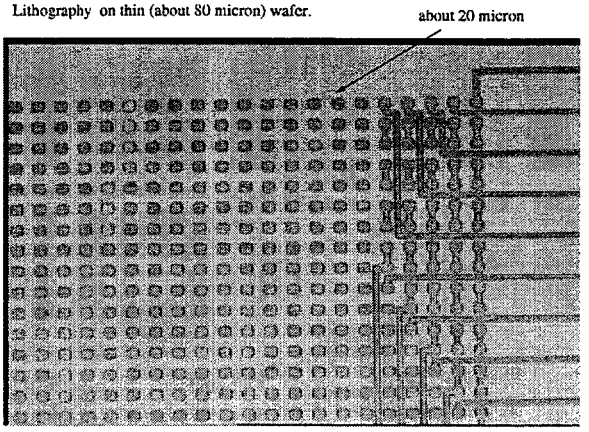

Figure 17: Lithography on a thin pixel. The smallest features are about 20 μm wide.

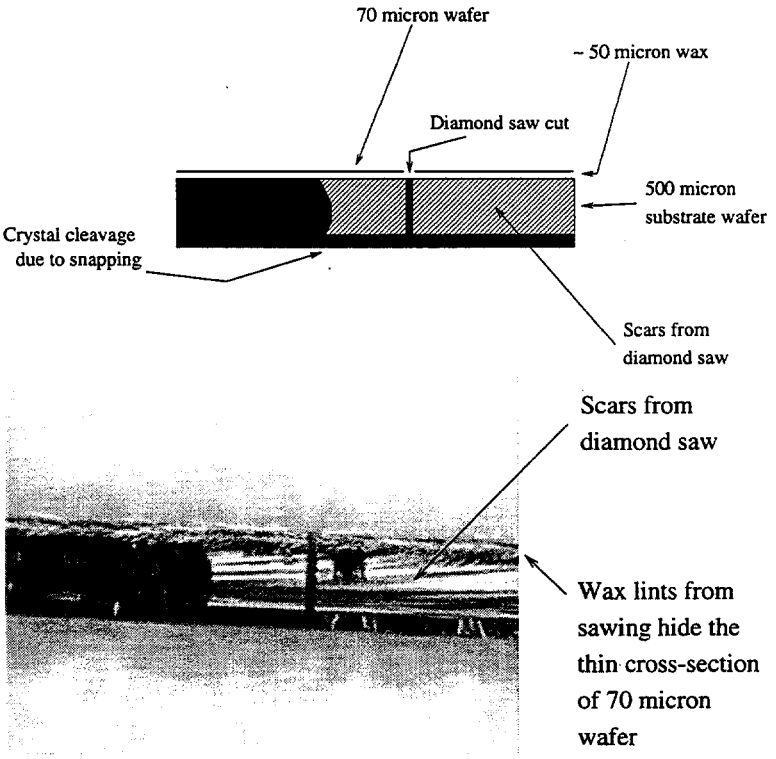

Figure 18: A cross-section of a diced thin wafer supported by a dummy wafer with wax.

Study of Radiation Damage to Honeywell RICMOS-IV SOI Transistors by Charged Hadrons [1]

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Abstract

We present preliminary results of an exposure of Honeywell RICMOS-IV SOI transistors to 2×10^{14} 63.3 MeV protons at the UCD cyclotron radiation test beam (27 Mrad (Si)). In terms of surface damage, this corresponds to almost twice the dose expected for the CMS pixel detector during its useful life at the LHC collider. The irradiated transistors include n-channel MOSFETs similar to the front-end transistors of a pixel readout we have designed for use at the next generation of detectors at hadron colliders. Data are presented on radiation-induced changes in threshold, transconductance, maximum voltage gain and noise for MOSFETs produced in a developmental SOI run. The preliminary results indicate that the readout front end would continue to function satisfactorily in the CMS radiation environment.

I. Introduction

The next generation of vertex detectors at colliders such as the Large Hadron Collider (LHC) at CERN will be subject to extreme radiation doses from high energy charged hadrons. For example, the inner part of the CMS pixel vertex detector, on which we are collaborating, is expected to be penetrated by of order 6×10^{14} such particles during its useful life [1], [2]. It is important to understand the limits of performance of the readout electronics under such conditions. For example, we have designed a pixel readout suitable for LHC applications [3]. The input transistor for the charge-sensitive amplifier is expected to be the component most sensitive to damage. In our design, this is an NMOS device with $w = 8.4\ \mu m$ and $l = 0.8\ \mu m$. A candidate radiation-hard technology for implementing the readout is the Honeywell SOI RICMOS-IV process [4]. This has been used successfully for radiation-hard digital circuitry, but its applicability for our analog use needs to be investigated.

For radiation tests, we have used Honeywell process monitor bars which include PMOS and NMOS transistors with nominal values of $w = 10\ \mu m$ and $l = 0.8\ \mu m$. The bars were specially processed to yield p-channel MOSFETs hard to a dose of 50 Mrad [5]. The gate oxide thickness was 15 nm, the barrier oxide thickness, 370 nm, and the effective gate length, 0.65 μm. We measured the $I - V$ characteristics and threshold shifts of these devices as a function of radiation dose and the noise in the frequency range 1-3 MHz for unirradiated devices and devices irradiated to 27 Mrad.

[1]Partially supported by US DOE contract DE-FG-03-91ER40674

II. Measurement Techniques

A. Irradiation and Testing

The devices were irradiated in the proton radiation test beam at the UC Davis Crocker Nuclear Laboratory (CNL) cyclotron [6]. The beam energy was 63.3 MeV. The fluence was monitored to 10% accuracy using a secondary emission monitor calibrated using a Faraday cup. The beam profile was approximately uniform over a 7 cm diameter, much larger than the devices under test. The dose rate was 2.3 Krad (Si)/s. Irradiation was done under bias ($V_{DS} = V_{GS} = 1\ V$ for NMOS and $V_{DS} = V_{GS} = -1\ V$ for PMOS devices) and in an argon atmosphere. Device parameters were measured with the beam off at 5 Mrad intervals using a Hewlett-Packard 4145B semiconductor parameter analyzer controlled by an Apple Macintosh computer running a LabVIEW [7] program.

B. Preliminary Noise Measurement

The input-referred noise amplitude in the frequency range 1-3 MHz was measured under operating conditions similar to that of the pixel readout front-end transistor. For this, a low-noise transimpedance amplifier calibrated using a signal generator and resistors was employed in conjunction with a Tektronix 2712 spectrum analyzer. Noise measurements were made approximately one month after the irradiation.

III. Results

A. Shift of Characteristic Curves and Thresholds

Changes under irradiation in the device performance ($I - V$ characteristics and thresholds) are shown in Figures 1 through 3. In general, larger changes were observed in the first 15 Mrad than in the reminder of the exposure.

B. Changes in Transconductance and Maximum Gain

Graphs of transconductance divided by drain current before irradiation and after the full 27 Mrad dose are shown for the n-channel and p-channel transistors in Figures 4 and 5, respectively. Figures 6 and 7 show corresponding results for maximum voltage gain, g_m/g_o. The front-end transistor in the pixel readout is an n-channel MOSFET and has an operating point in the neighborhood of 10 μA. Here, the transconductance falls by approximately 20% and the maximum gain by 40% of the original values.

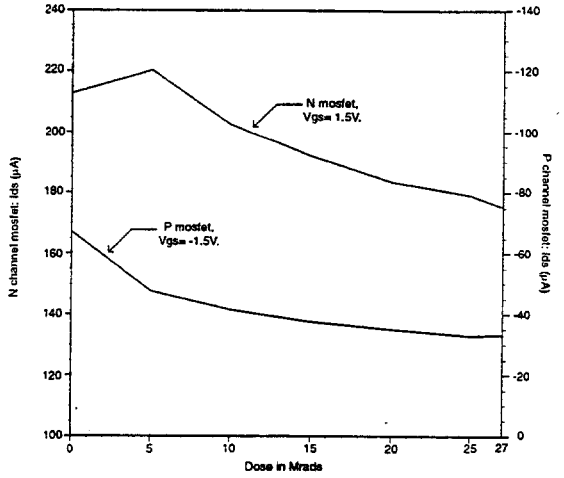

Figure 1: Typical shifts of I_{DS} for fixed V_{GS} due to irradiation.

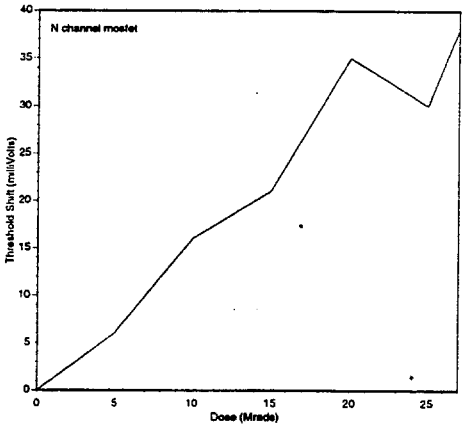

Figure 2: Threshold shift for the NMOS device as a function of dose.

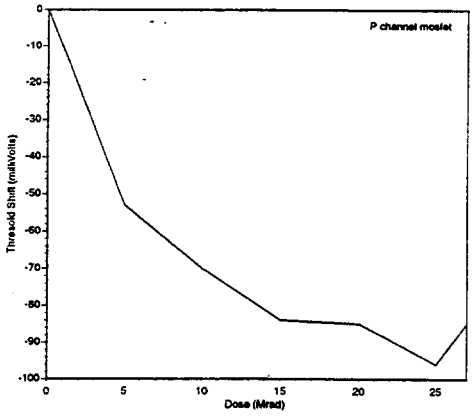

Figure 3: Threshold shift for the PMOS device as a function of dose.

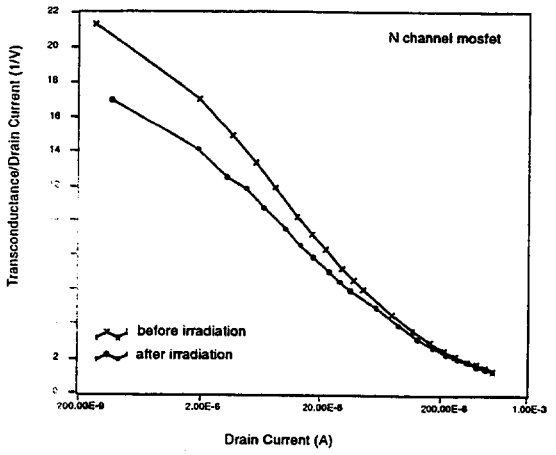

Figure 4: Plots of g_m/I_D before and after a dose of 27 Mrad (Si) for the n-channel transistor.

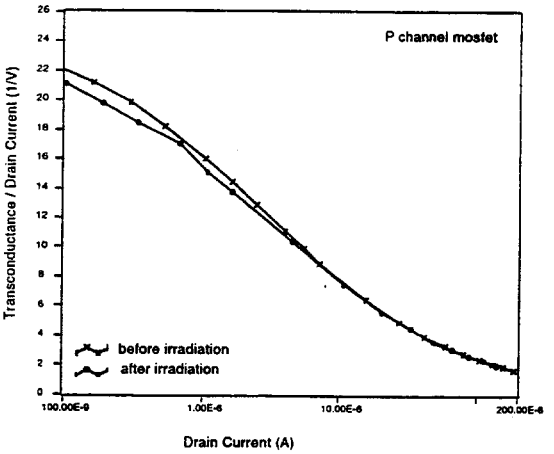

Figure 5: Plots of g_m/I_D before and after a dose of 27 Mrad (Si) for the p-channel transistor.

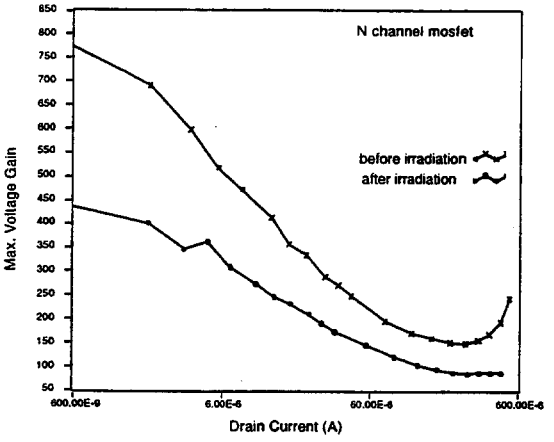

Figure 6: Plots of $A_v(max) = g_m/g_o$ before and after a dose of 27 Mrad (Si) for the n-channel transistor.

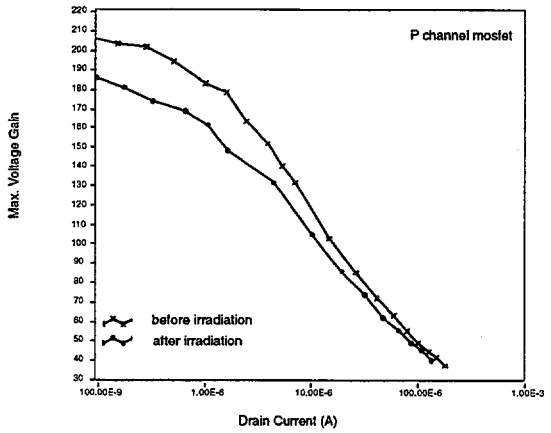

Figure 7: Plots of $A_v(max) = g_m/g_o$ before and after a dose of 27 Mrad (Si) for the p-channel transistor.

C. *Preliminary Noise Measurement*

Noise measurements before and after irradiation at a center frequency of 2 MHz are listed in Table 1.

Table 1
Noise Measured at 2 MHz

FET (*type*)	Dose ($Mrad$)	g_m (μS)	v_N ($nV/\sqrt{Hz}$)	v_{N_0} ($nV/\sqrt{Hz}$)
NMOS	0	140	20	9
NMOS	27	125	40	9
PMOS	0	88	22	11
PMOS	27	95	32	11

The measurement conditions correspond to the operating point of the input transistor, $I_D = 10\ \mu A$ and $V_{DS} = 500\ mV$. The spectra in the interval 1-3 MHz were observed to be flat. In Table 1, v_N is the measured rms noise voltage per $\sqrt{\text{Hz}}$. An estimate of the thermal noise expected from the channel resistance, $v_{N_0} = \sqrt{(0.67)4kT/g_m}$, is included for comparison. Prior to irradiation, v_N is approximately twice v_{N_0} for both the n- and the p-channel devices. After a dose of 27 Mrad, there is a further increase of 100% in v_N for the n-channel device and 50% for the p-channel.

These effects may be understood in the context of a recent model for excess apparent white noise in SOI MOSFETs proposed by F. Faccio *et al.* [8], in which the excess comes from thermal noise associated with the body resistance, increasing as the body resistance increases. The input-referred noise amplitude was observed to change as the body resistance was varied via the body or backgate bias. This provides a possible method for reducing the noise. In our case, the body resistance can vary in response to radiation-induced positive charge in the buried oxide. We are currently carrying out more detailed noise measurements and investigating these effects in the Honeywell devices.

IV. Conclusions

Our preliminary conclusion is that the pixel front-end would continue to operate in the LHC environment. Noise remains a primary concern since the discriminator threshold needs to be approximately five times the expected noise level to prevent overloading the data acquisition system with random hits. More detailed noise measurements and circuit simulations are currently underway, including measurements of the effects of body and backgate biasing on noise.

V. Acknowledgements

We are grateful to Dr. C. Castaneda of the UC Davis Crocker Nuclear Laboratory (CNL) for assistance with the test beam and to CNL for granting development time for this run. We wish to thank the UCD Physics Department Electrical Engineer, B. Holbrook, for developing the noise measurement apparatus. It is a pleasure to acknowledge useful comments, information and suggestions from S.T. Liu and M. Flanery of the Honeywell Solid State Electronics Center and from P. Seller.

VI. References

[1] *The Compact Muon Solenoid Technical Proposal: CERN/LHCC 94-38, 1994.*

[2] *The CMS Tracker Project Technical Design Report: CERN/LHCC 98-6, 1998.*

[3] G.P. Grim, R.L. Lander, S. Mani, S. Gaalema, and W. Feng, "An analog front-end for the CMS pixel detector," *Proceedings of the Workshop on Electronics for LHC Experiments, Balatonfüred, Hungary: CERN-LHCC-96-39, 1996* pp. 438-441.

[4] Honeywell Solid State Electronics Center, Minneapolis, Minnesota 55441.

[5] S.T. Liu, T. Bradow, W.C. Jenkins and H.L. Hughes, "Further Radiation Hardened SOI CMOS Technologies," *Proceedings of the Third Workshop on Electronics for LHC Experiments, London, UK: CERN-LHCC-97-60, 1997* pp. 130-133.

[6] The proton radiation test beam at CNL was set up and instrumented through a joint effort of CNL and the U.S. Naval Research Laboratory.

[7] National Instruments Corporation, 6504 Bridge Point Parkway, Austin, TX 78730-5039.

[8] F. Faccio, F. Anghinolfi, E.H.M. Heijne, P. Jarron and S. Cristoloveanu, "Noise Contribution of the Body Resistance in Partially-Depleted SOI MOSFET's," *IEEE Trans. Electron Devices, Vol. 45, 1998* pp. 1033-1038.